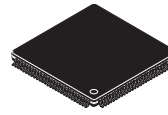
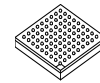




## MCF52277



LQFP-176  
24 mm x 24 mm



MAPBGA-196  
15mm x 15mm

# MCF5227x ColdFire® Microprocessor Data Sheet

### Features

- Version 2 ColdFire® Core with EMAC
- Up to 159 Dhrystone 2.1 MIPS @ 166.67 MHz
- 8 Kbytes configurable cache (instruction only, data only, or split instruction/data)
- 128 Kbytes internal SRAM
- Support for booting from SPI-compatible flash, EEPROM, and FRAM devices
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- 16 channel DMA controller
- 16- or 32-bit SDR/DDR controller
- USB 2.0 On-the-Go controller
- Liquid crystal display controller with support up to 800 × 600 pixels
- ADC and touchscreen controller
- FlexCAN module
- 4 32-bit timers with DMA support
- DMA supported serial peripheral interface (DSPI)
- 3 UARTs
- I<sup>2</sup>C bus interface
- Synchronous serial interface (SSI)
- Plus-width modulator (PWM)
- Real-time clock (RTC)
- Two programmable interrupt controllers (PIT)

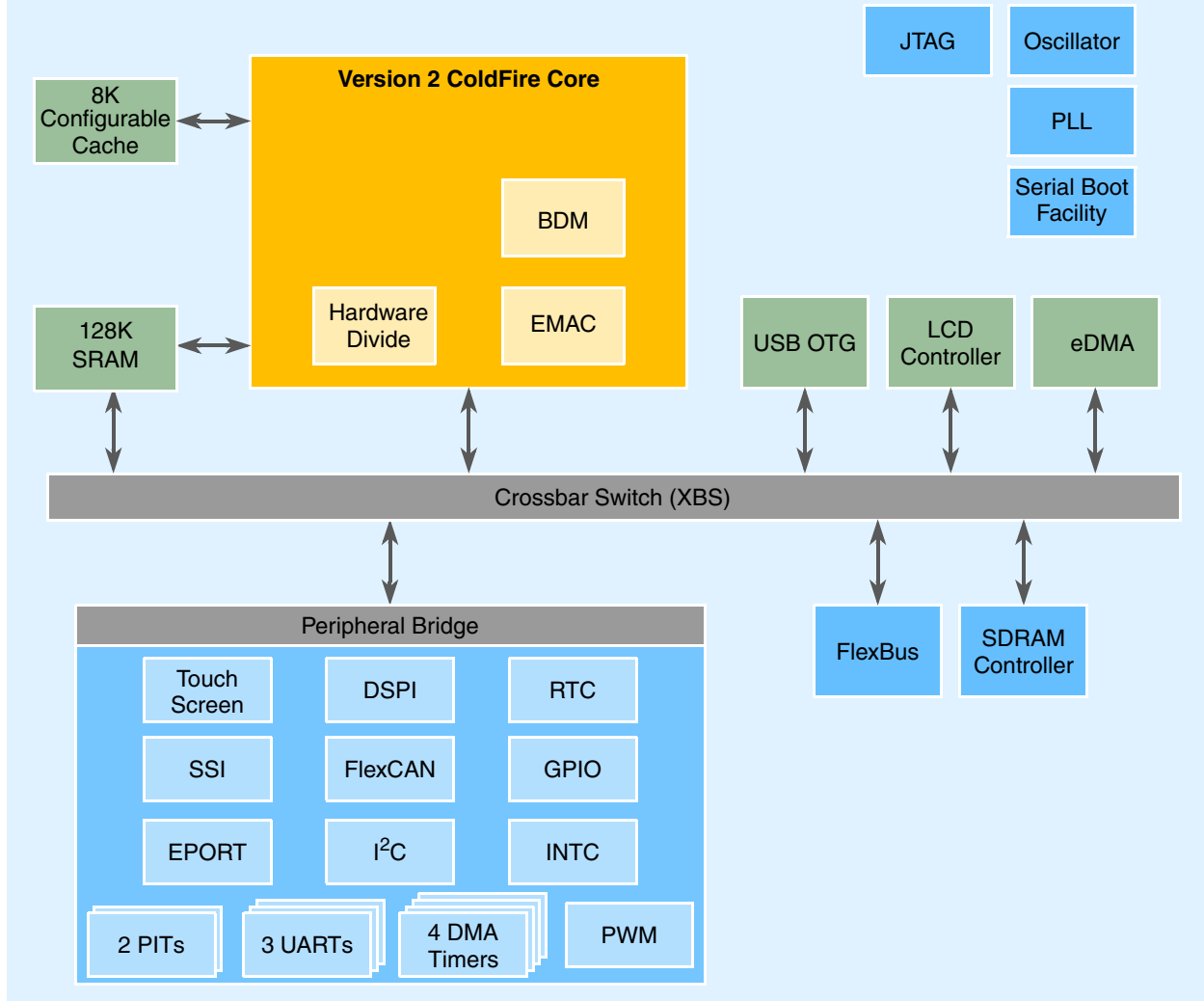
This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**Preliminary—Subject to Change Without Notice**

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**MCF52277**

**LEGEND**

<b>BDM</b>	– Background debug module	<b>LCD</b>	– Liquid-crystal display
<b>DSPI</b>	– DMA serial peripheral interface	<b>PIT</b>	– Programmable interrupt timer
<b>eDMA</b>	– Enhanced direct memory access	<b>PLL</b>	– Phase locked loop module
<b>EMAC</b>	– Enhance multiply-accumulate unit	<b>PWM</b>	– Pulse-width modulator
<b>EPORT</b>	– Edge port module	<b>RTC</b>	– Real time clock
<b>GPIO</b>	– General Purpose Input/Output Module	<b>SSI</b>	– Synchronous Serial Interface
<b>I<sup>2</sup>C</b>	– Inter-Integrated Circuit	<b>UART</b>	– Universal asynchronous receiver/transmitter
<b>INTC</b>	– Interrupt controller	<b>USB OTG</b>	– Universal Serial Bus On-the-Go controller
<b>JTAG</b>	– Joint Test Action Group interface		

**Figure 1. MCF52277 Block Diagram**

# 1 MCF5227x Family Comparison

The following table compares the various device derivatives available within the MCF5227x family.

**Table 1. MCF5227x Family Configurations**

Module	MCF52274	MCF52277
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•
Core (System) Clock	up to 120 MHz	up to 166.67 MHz
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 60 MHz	up to 83.33 MHz
Performance (Dhrystone/2.1 MIPS)	up to 114	up to 159
Static RAM (SRAM)	128 Kbytes	
Configurable Cache	8 Kbytes	
ASP Touchscreen Controller	•	•
LCD Controller	12-bit color	18-bit color
USB 2.0 On-the-Go	•	•
FlexBus External Interface	•	•
SDR/DDR SDRAM Controller	•	•
FlexCAN 2.0B communication module	•	•
Real Time Clock	•	•
Watchdog Timer	•	•
16-channel Direct Memory Access (DMA)	•	•
Interrupt Controllers (INTC)	1	1
Synchronous Serial Interface (SSI)	•	•
I <sup>2</sup> C	•	•
DSPI	•	•
UARTs	3	3
32-bit DMA Timers	4	4
Periodic Interrupt Timers (PIT)	2	2
PWM Module	•	•
Edge Port Module (EPORT)	•	•
General Purpose I/O Module (GPIO)	•	•
JTAG - IEEE <sup>®</sup> 1149.1 Test Access Port	•	•
Package	176 LQFP	196 MAPBGA

## 2 Ordering Information

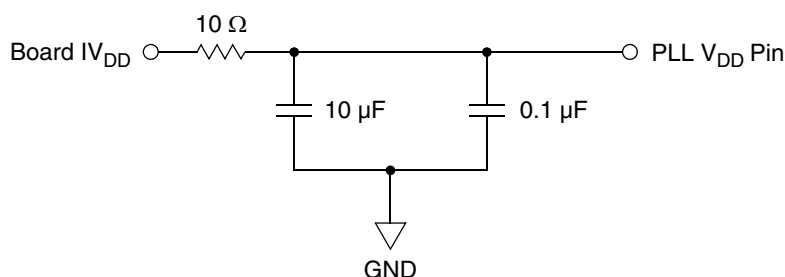
Table 2. Orderable Part Numbers

Freescall Part Number	Description	Package	Speed	Temperature
MCF52274CLU120	MCF52274 RISC Microprocessor	176 LQFP	120 MHz	-40° to +85° C
MCF52277CVM160	MCF52277 RISC Microprocessor	196 MAPBGA	166.67 MHz	-40° to +85° C

## 3 Hardware Design Considerations

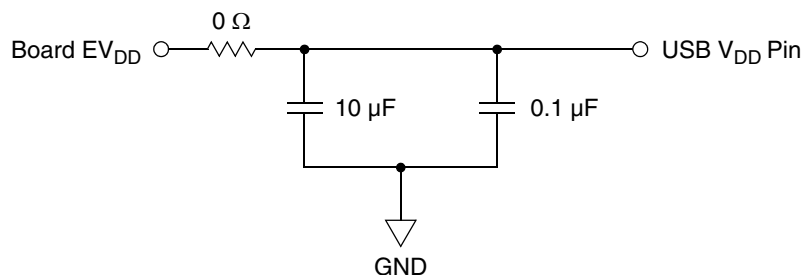
### 3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog  $V_{DD}$  pins. The filter shown in Figure 2 should be connected between the board  $V_{DD}$  and the PLL $V_{DD}$  pins. The resistor and capacitors should be placed as close to the dedicated PLL $V_{DD}$  pin as possible.

Figure 2. System PLL  $V_{DD}$  Power Filter

### 3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 3 should be connected between the board  $E_{VDD}$  and the USB $V_{DD}$  pin. The resistor and capacitors should be placed as close to the dedicated USB $V_{DD}$  pin as possible.

Figure 3. USB  $V_{DD}$  Power Filter

#### NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

### 3.3 ADC Power Filtering

To minimize noise, an external filter is required for the ADCV<sub>DD</sub> power pin. The filter shown in Figure 4 should be connected between the board EV<sub>DD</sub> and the ADCV<sub>DD</sub> pin. The resistor and capacitors should be placed as close to the dedicated ADCV<sub>DD</sub> pin as possible.

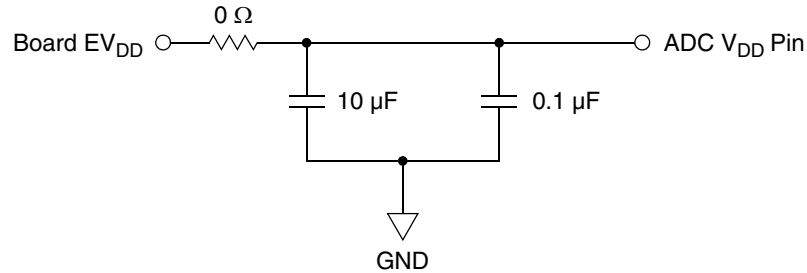


Figure 4. ADC V<sub>DD</sub> Power Filter

### 3.4 Supply Voltage Sequencing

The relationship between SDV<sub>DD</sub> and EV<sub>DD</sub> is non-critical during power-up and power-down sequences. Both SDV<sub>DD</sub> (2.5V or 3.3V) and EV<sub>DD</sub> are specified relative to IV<sub>DD</sub>.

#### 3.4.1 Power Up Sequence

If EV<sub>DD</sub>/SDV<sub>DD</sub> are powered up with IV<sub>DD</sub> at 0 V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV<sub>DD</sub>/SDV<sub>DD</sub> to be in a high impedance state. There is no limit on how long after EV<sub>DD</sub>/SDV<sub>DD</sub> powers up before IV<sub>DD</sub> must be powered up. IV<sub>DD</sub> should not lead the EV<sub>DD</sub>, SDV<sub>DD</sub> or PLLV<sub>DD</sub> by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

#### 3.4.2 Power Down Sequence

If IV<sub>DD</sub>/PLLV<sub>DD</sub> are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV<sub>DD</sub> and PLLV<sub>DD</sub> power down before EV<sub>DD</sub> or SDV<sub>DD</sub> must power down. IV<sub>DD</sub> should not lag EV<sub>DD</sub>, SDV<sub>DD</sub>, or PLLV<sub>DD</sub> going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV<sub>DD</sub>/PLLV<sub>DD</sub> to 0 V.
2. Drop EV<sub>DD</sub>/SDV<sub>DD</sub> supplies.

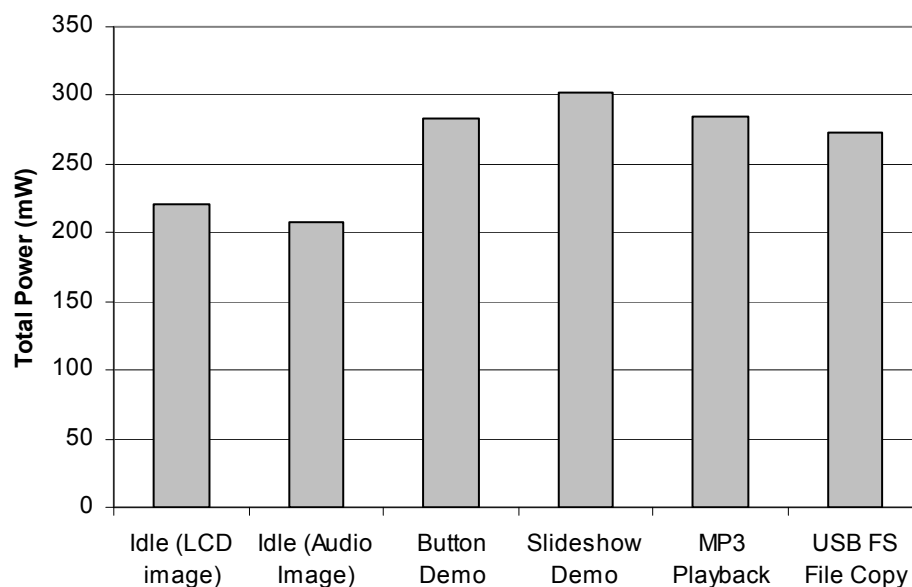
### 3.5 Power Consumption Specifications

All application power consumption data is lab data measured on an M52277EVB running the Freescale Linux BSP.

**Table 3. MCF52277 Application Power Consumption<sup>1</sup>**

Core Freq.		Idle (LCD image)	Idle (audio image)	Button Demo	Slideshow Demo	MP3 Playback	USB FS File Copy	Units
160 MHz	$IV_{DD}$	61.4	59.2	84.7	96.5	89.2	89.5	mA
	$EV_{DD}$	28.87	25.73	35.3	34.6	33.46	29.86	
	$SDV_{DD}$	18.8	18.57	21.8	23.9	22.66	22.2	
	<b>Total Power</b>	<b>221.211</b>	<b>207.135</b>	<b>282.78</b>	<b>301.95</b>	<b>285.006</b>	<b>272.748</b>	<b>mW</b>

<sup>1</sup> All voltage rails at nominal values:  $IV_{DD} = 1.5$  V,  $EV_{DD} = 3.3$  V, and  $SDV_{DD} = 1.8$  V.



**Figure 5. Power Consumption in Various Applications**

All current consumption data is lab data measured on a single device using an evaluation board. Table 4 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

**Table 4. Current Consumption in Low-Power Modes<sup>1,2</sup>**

Mode	Voltage Supply	System Frequency				
		80MHz	64MHz	48MHz	32MHz	4MHz (LIMP mode)
RUN	$IV_{DD}$ (mA)	75.1	62.7	49.2	36.6	3.5
	Power (mW)	112.65	94.05	73.80	54.90	5.25
WAIT	$IV_{DD}$ (mA)	61.9	52.8	42.0	31.7	2.9
	Power (mW)	92.85	79.20	63.00	47.55	4.35

Table 4. Current Consumption in Low-Power Modes<sup>1,2</sup> (continued)

Mode	Voltage Supply	System Frequency				
		80MHz	64MHz	48MHz	32MHz	4MHz (LIMP mode)
DOZE	$I_{DD}$ (mA)	57.0	48.8	38.9	29.7	2.7
	Power (mW)	85.50	73.20	58.35	44.55	4.05
STOP 0	$I_{DD}$ (mA)	16.1	15.1	13.4	12.5	1.3
	Power (mW)	24.15	22.65	20.10	18.75	1.95
STOP 1	$I_{DD}$ (mA)	15.9	14.9	13.2	12.4	1.3
	Power (mW)	23.85	22.35	19.80	18.60	1.95
STOP 2	$I_{DD}$ (mA)	1.8	1.8	1.8	1.8	1.3
	Power (mW)	2.70	2.70	2.70	2.70	1.95
STOP 3	$I_{DD}$ (mA)	0.5	0.5	0.5	0.5	0.5
	Power (mW)	0.75	0.75	0.75	0.75	0.75

<sup>1</sup> All values are measured on an M52277EVB with nominal core voltage ( $I_{DD} = 1.5\text{ V}$ ). Tests performed at room temperature. All peripheral clocks on prior to entering low-power mode

<sup>2</sup> Refer to the Power Management chapter in the *MCF52277 Reference Manual* for more information on low-power modes.

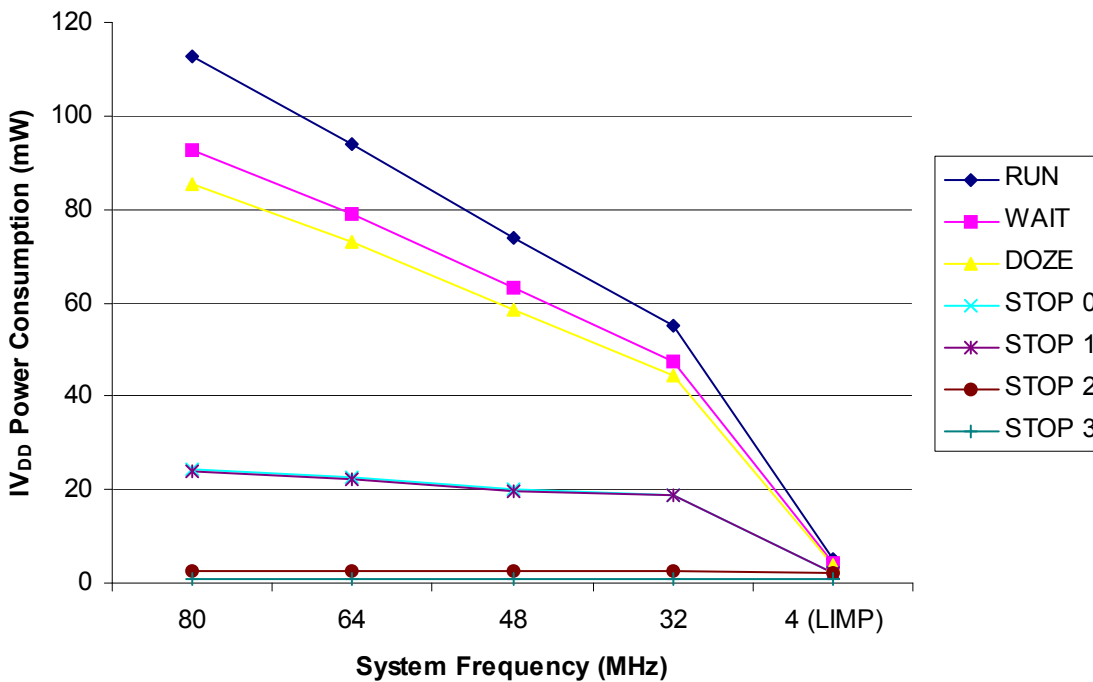


Figure 6.  $I_{DD}$  Power Consumption in Low-Power Modes



## 4 Pin Assignments and Reset States

### 4.1 Signal Multiplexing

The following table lists all the MCF5227x pins grouped by function. The direction column is the direction for the primary function of the pin only. Refer to [Section 4, “Pin Assignments and Reset States,”](#) for package diagrams. For a more detailed discussion of the MCF5227x signals, consult the *MCF52277 Reference Manual* (MCF52277RM).

#### NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB\_A23), while designations for multiple signals within a group use brackets (i.e., FB\_A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

#### NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO will default to their GPIO functionality. See [Table 5](#) for a list of the exceptions.

**Table 5. Special-Case Default Signal Functionality**

Pin	Default Signal
$\overline{\text{FB\_BE/BWE}}[3:0]$	$\overline{\text{FB\_BE/BWE}}[3:0]$
$\overline{\text{FB\_CS}}[3:0]$	$\overline{\text{FB\_CS}}[3:0]$
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$
$\overline{\text{FB\_R/W}}$	$\overline{\text{FB\_R/W}}$
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$

**Table 6. MCF5227x Signal Information and Muxing**

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U) <sup>1</sup> Pull-down (D)	Direction <sup>2</sup>	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
<b>Reset</b>								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	103	J11
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	102	K11
<b>Clock</b>								
EXTAL	—	—	—	—	I	EVDD	106	F14
XTAL	—	—	—	U <sup>3</sup>	O	EVDD	105	G14
<b>Mode Selection</b>								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	110, 109	G10, H10

Table 6. MCF5227x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U) <sup>1</sup> Pull-down (D)	Direction <sup>2</sup>	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
<b>FlexBus</b>								
FB_A[23:22]	—	$\overline{\text{FB\_CS}}[5:4]$	—	—	O	SDVDD	143, 142	C11, D11
FB_A[21:16]	—	—	—	—	O	SDVDD	141–139, 137–135	A12, B12, C12, B13, A13, A14
FB_A[15:14]	—	SD_BA[1:0]	—	—	O	SDVDD	131, 130	B14, C13
FB_A[13:11]	—	SD_A[13:11]	—	—	O	SDVDD	129–127	C14, D12, D13
FB_A10	—	—	—	—	O	SDVDD	126	D14
FB_A[9:0]	—	SD_A[9:0]	—	—	O	SDVDD	125–116	E11–E14, F11–F13, G11, G12, H11
FB_D[31:16]	—	SD_D[31:16]	—	—	I/O	SDVDD	30–37, 49–56	J4, K1–K4, L1–L3, M3, N3, P3, M4, N4, P4, L5, M5
FB_D[15:0]	—	FB_D[31:16]	—	—	I/O	SDVDD	19–26, 60–67	G1–G4, H1–H4, M6, N6, P6, L7, M7, N7, P7, L8
FB_CLK	—	—	—	—	O	SDVDD	42	P1
$\overline{\text{FB\_BE/BWE}}[3:0]$	PBE[3:0]	SD_DQM[3:0]	—	—	O	SDVDD	29, 57, 27, 59	J3, N5, J1, L6
$\overline{\text{FB\_CS}}[3:2]$	PCS[3:2]	—	—	—	O	SDVDD	—	B11, A11
$\overline{\text{FB\_CS}}1$	PCS1	$\overline{\text{SD\_CS}}1$	—	—	O	SDVDD	144	D10
$\overline{\text{FB\_CS}}0$	PCS0	—	—	—	O	SDVDD	145	C10
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	SDVDD	69	N8
$\overline{\text{FB\_TA}}$	PFBCTL2	—	—	U	I	SDVDD	115	H12
$\overline{\text{FB\_R/W}}$	PFBCTL1	—	—	—	O	SDVDD	68	M8
$\overline{\text{FB\_TS}}$	PFBCTL0	$\overline{\text{DACK}}0$	—	—	O	SDVDD	15	F4
<b>SDRAM Controller</b>								
SD_A10	—	—	—	—	O	SDVDD	46	L4
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	47	N2
SD_CKE	—	—	—	—	O	SDVDD	17	F2
SD_CLK	—	—	—	—	O	SDVDD	40	M1
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	41	N1
$\overline{\text{SD\_CS}}0$	—	—	—	—	O	SDVDD	18	F1
SD_DQS[3:2]	—	—	—	—	I/O	SDVDD	28, 58	J2, P5
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	48	P2
SD_SDR_DQS	—	—	—	—	O	SDVDD	38	M2

Table 6. MCF5227x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U) <sup>1</sup> Pull-down (D)	Direction <sup>2</sup>	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
SD_WE	—	—	—	—	O	SDVDD	16	F3
<b>External Interrupts Port<sup>4</sup></b>								
IRQ7	PIRQ7	—	—	—	I	EVDD	162	D7
IRQ4	PIRQ4	DREQ0	DSPI_PCS4	5	I	EVDD	161	C7
IRQ1	PIRQ1	USB_CLKIN	SSI_CLKIN	—	I	EVDD	160	B7
<b>LCD Controller<sup>6</sup></b>								
LCD_D[17:16] <sup>6</sup>	PLCDDH[1:0]	LCD_D[11:10]	—	—	O	EVDD	9, 8	E3, E4
LCD_D[15:14] <sup>6</sup>	PLCDDM[7:6]	LCD_D[9:8]	—	—	O	EVDD	7, 6	D1, D2
LCD_D13	PLCDDM5	CANTX	—	—	O	EVDD	—	C1
LCD_D12	PLCDDM4	CANRX	—	—	O	EVDD	—	C2
LCD_D[11:8] <sup>6</sup>	PLCDDM[3:0]	LCD_D[7:4]	—	—	O	EVDD	5–2	D3, C3, D4, B1
LCD_D7	PLCDDL7	PWM7	—	—	O	EVDD	—	B2
LCD_D6	PLCDDL6	PWM5	—	—	O	EVDD	—	A1
LCD_D[5:2] <sup>6</sup>	PLCDDL[5:2]	LCD_D[3:0]	—	—	O	EVDD	175–172	A2, A3, B3, A4
LCD_D1	PLCDDL1	PWM3	—	—	O	EVDD	—	B4
LCD_D0	PLCDDL0	PWM1	—	—	O	EVDD	—	C4
LCD_ACD/ LCD_OE	PLCDCTL3	LCD_SPL_SPR	—	—	O	EVDD	169	B5
LCD_FLM/ LCD_VSYNC	PLCDCTL2	—	—	—	O	EVDD	10	E2
LCD_LP/ LCD_HSYNC	PLCDCTL1	—	—	—	O	EVDD	11	E1
LCD_LSCLK	PLCDCTL0	—	—	—	O	EVDD	170	A5
<b>USB On-the-Go</b>								
USB_DM	—	—	—	—	O	USB VDD	149	A9
USB_DP	—	—	—	—	O	USB VDD	150	A10
<b>Real Time Clock</b>								
RTC_EXTAL	—	—	—	—	I	EVDD	100	J14
RTC_XTAL	—	—	—	—	O	EVDD	99	K14

Table 6. MCF5227x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U) <sup>1</sup> Pull-down (D)	Direction <sup>2</sup>	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
<b>ADC</b>								
ADC_IN[7:0]	—	—	—	—	I	VDD_ADC	82–85, 87–90	P12, N12, P13, N13, P14, N14, M13, M14
ADC_REF	—	—	—	—	I	VDD_ADC	86	M12
<b>I<sup>2</sup>C</b>								
I2C_SCL	PI2C1	CANTX	U2TXD	U	I/O	EVDD	168	C5
I2C_SDA	PI2C0	CANRX	U2RXD	U	I/O	EVDD	167	D5
<b>DSPI<sup>7</sup></b>								
DSPI_PCS0/ <u>SS</u>	PDSPI3	<u>U2RTS</u>	—	U	I/O	EVDD	152	B9
DSPI_SIN	PDSPI2	U2RXD	SBF_DI	8	I	EVDD	155	D8
DSPI_SOUT	PDSPI1	U2TXD	SBF_D0	—	O	EVDD	154	D9
DSPI_SCK	PDSPI0	<u>U2CTS</u>	SBF_CK	—	I/O	EVDD	153	C9
<b>UARTs</b>								
<u>U1CTS</u>	PUART7	SSI_BCLK	LCD_CLS	—	I	EVDD	156	C8
<u>U1RTS</u>	PUART6	SSI_FS	LCD_PS	—	O	EVDD	157	B8
U1RXD	PUART5	SSI_RXD	—	—	I	EVDD	158	A8
U1TXD	PUART4	SSI_TXD	—	—	O	EVDD	159	A7
<u>U0CTS</u>	PUART3	DT1OUT	USB_VBUS_EN	—	I	EVDD	97	K12
<u>U0RTS</u>	PUART2	DT1IN	USB_VBUS_OC	—	O	EVDD	98	J12
U0RXD	PUART1	CANRX	—	—	I	EVDD	96	K13
U0TXD	PUART0	CANTX	—	—	O	EVDD	95	L12
<b>DMA Timers</b>								
DT3IN	PTIMER3	DT3OUT	SSI_MCLK	—	I	EVDD	163	D6
DT2IN/ <u>SBF_CS</u> <sup>7</sup>	PTIMER2	DT2OUT	DSPI_PCS2	—	I	EVDD	164	C6
DT1IN	PTIMER1	DT1OUT	LCD_CONTRAST	—	I	EVDD	165	B6
DT0IN	PTIMER0	DT0OUT	LCD_REV	—	I	EVDD	166	A6
<b>BDM/JTAG<sup>9</sup></b>								
PST[3:0]	—	—	—	—	O	EVDD	—	L9, M9, N9, P9
DDATA[3:0]	—	—	—	—	O	EVDD	—	L10, M10, N10, P10
ALLPST	—	—	—	—	O	EVDD	76	—

Table 6. MCF5227x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U) <sup>1</sup> Pull-down (D)	Direction <sup>2</sup>	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
JTAG_EN	—	—	—	D	I	EVDD	79	K10
PSTCLK	—	TCLK	—	U	O	EVDD	74	P8
DSI	—	TDI	—	U	I	EVDD	78	M11
DSO	—	TDO	—	—	O	EVDD	81	L11
$\overline{\text{BKPT}}$	—	TMS	—	U	I	EVDD	80	N11
DSCLK	—	$\overline{\text{TRST}}$	—	U	I	EVDD	77	P11
<b>Test</b>								
TEST	—	—	—	D	I	EVDD	134	E10
<b>Power Supplies</b>								
IVDD	—	—	—	—	—	—	39, 75, 114, 138, 171	K5, F10, E5, J10
EVDD	—	—	—	—	—	—	12, 72, 73, 94, 111, 148, 176	E6, E7, F5, F6, G5, H9, J9, K8, K9
SD_VDD	—	—	—	—	—	—	14, 43, 44, 70, 113, 132, 146	E8, E9, F9, G9, H5, J5, J6, K6, K7
VDD_OSC	—	—	—	—	—	—	108	G13
VDD_PLL	—	—	—	—	—	—	104	H14
VDD_USB	—	—	—	—	—	—	151	B10
VDD_RTC	—	—	—	—	—	—	101	J13
VDD_ADC	—	—	—	—	—	—	91	L13
VSS	—	—	—	—	—	—	1, 13, 45, 71, 93, 112, 133, 147	F7, F8, G6–G8, H6–H8, J7, J8
VSS_OSC	—	—	—	—	—	—	107	H13
VSS_ADC	—	—	—	—	—	—	92	L14

<sup>1</sup> Pull-ups are generally only enabled on pins with their primary function, except as noted.

<sup>2</sup> Refers to pin's primary function.

<sup>3</sup> Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

<sup>4</sup> GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

<sup>5</sup> Pull-up when  $\overline{\text{DREQ}}$  controls the pin.

<sup>6</sup> The 176 LQFP device only supports a 12-bit LCD data bus.

<sup>7</sup> DSPI or SBF signal functionality is controlled by  $\overline{\text{RESET}}$ . When asserted, these pins are configured for serial boot; when negated, the pins are configured for DSPI.

<sup>8</sup> Pull-up when the serial boot facility (SBF) controls the pin.

<sup>9</sup> If JTAG\_EN is asserted, these pins default to alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

## 4.2 Pinout—176 LQFP

The pinout for the MCF52274 package is shown below.

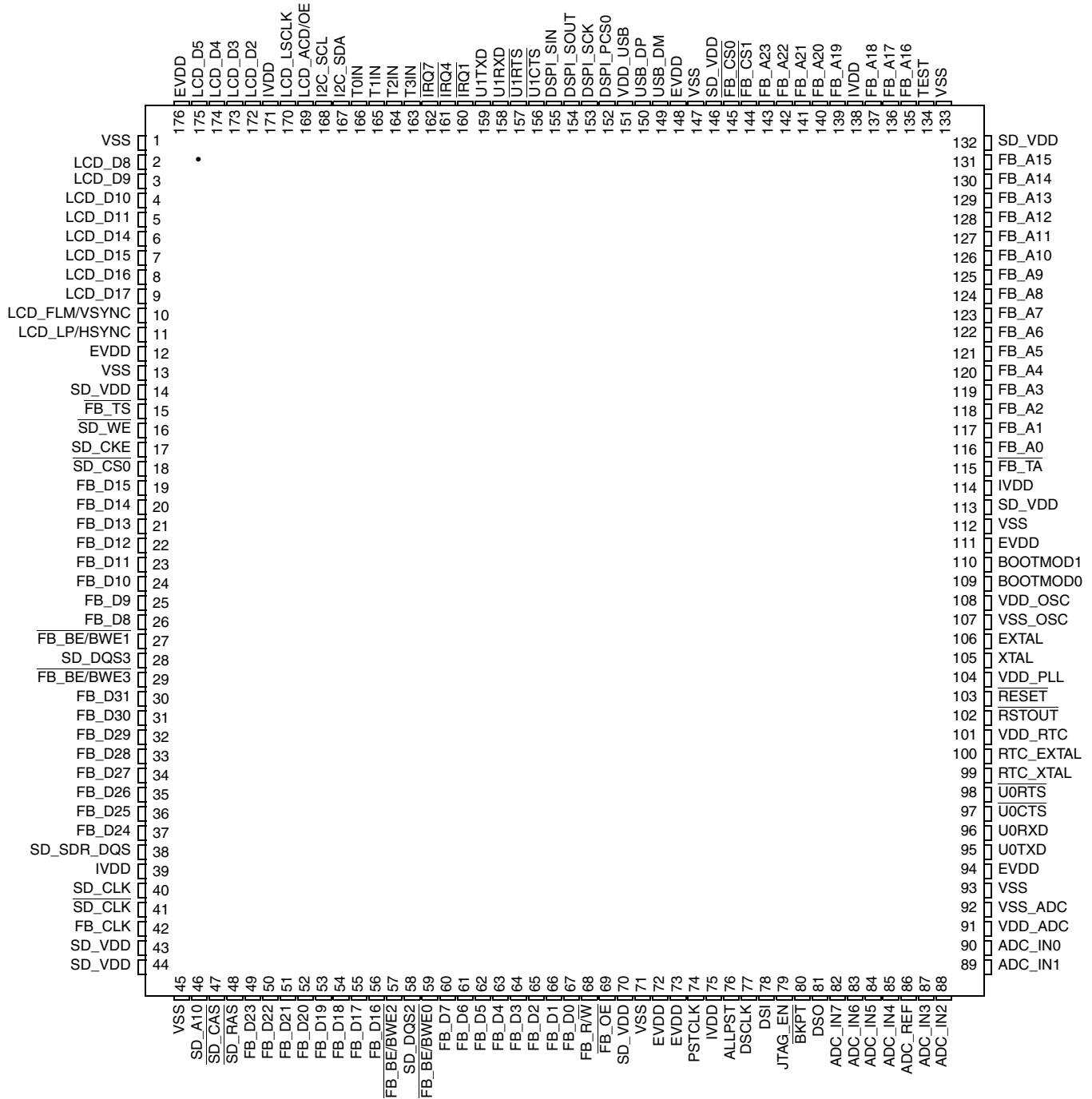


Figure 7. MCF52274 Pinout (176 LQFP)

### 4.3 Pinout—196 MAPBGA

The pinout for the MCF52277 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	LCD_D6	LCD_D5	LCD_D4	LCD_D2	LCD_LSCLK	T0IN	U1TXD	U1RXD	USB_DM	USB_DP	$\overline{\text{FB\_CS2}}$	FB_A21	FB_A17	FB_A16	A
B	LCD_D8	LCD_D7	LCD_D3	LCD_D1	LCD_ACD/OE	T1IN	$\overline{\text{IRQ\_1}}$	$\overline{\text{U1RTS}}$	DSPI_PCS0	VDD_USB	$\overline{\text{FB\_CS3}}$	FB_A20	FB_A18	FB_A15	B
C	LCD_D13	LCD_D12	LCD_D10	LCD_D0	I2C_SCL	T2IN	$\overline{\text{IRQ\_4}}$	$\overline{\text{U1CTS}}$	DSPI_SCK	$\overline{\text{FB\_CS0}}$	FB_A23	FB_A19	FB_A14	FB_A13	C
D	LCD_D15	LCD_D14	LCD_D11	LCD_D9	I2C_SDA	T3IN	$\overline{\text{IRQ\_7}}$	DSPI_SIN	DSPI_SOUT	$\overline{\text{FB\_CS1}}$	FB_A22	FB_A12	FB_A11	FB_A10	D
E	LCD_LP/HSYNC	LCD_FLM/VSYNC	LCD_D17	LCD_D16	IVDD	EVDD	EVDD	SDVDD	SDVDD	TEST	FB_A9	FB_A8	FB_A7	FB_A6	E
F	$\overline{\text{SD\_CS0}}$	SD_CKE	$\overline{\text{SD\_WE}}$	$\overline{\text{FB\_TS}}$	EVDD	EVDD	VSS	VSS	SDVDD	IVDD	FB_A5	FB_A4	FB_A3	EXTAL	F
G	FB_D15	FB_D14	FB_D13	FB_D12	EVDD	VSS	VSS	VSS	SDVDD	BOOT_MOD1	FB_A2	FB_A1	VDD_OSC	XTAL	G
H	FB_D11	FB_D10	FB_D9	FB_D8	SDVDD	VSS	VSS	VSS	EVDD	BOOT_MOD0	FB_A0	$\overline{\text{FB\_TA}}$	VSS_OSC	VDD_PLL	H
J	$\overline{\text{FB\_BE/BWE1}}$	SD_DQS3	$\overline{\text{FB\_BE/BWE3}}$	FB_D31	SDVDD	SDVDD	VSS	VSS	EVDD	IVDD	RESET	$\overline{\text{U0RTS}}$	VDD_RTC	RTC_EXTAL	J
K	FB_D30	FB_D29	FB_D28	FB_D27	IVDD	SDVDD	SDVDD	EVDD	EVDD	JTAG_EN	$\overline{\text{RSTOUT}}$	$\overline{\text{U0CTS}}$	U0RXD	RTC_XTAL	K
L	FB_D26	FB_D25	FB_D24	SD_A10	FB_D17	$\overline{\text{FB\_BE/BWE0}}$	FB_D4	FB_D0	PST3	DDATA3	TDO	U0TXD	VDD_ADC	VSS_ADC	L
M	SD_CLK	SD_SDR_DQS	FB_D23	FB_D20	FB_D16	FB_D7	FB_D3	FB_R $\overline{\text{W}}$	PST2	DDATA2	TDI	ADC_REF	ADC_IN1	ADC_IN0	M
N	$\overline{\text{SD\_CLK}}$	$\overline{\text{SD\_CAS}}$	FB_D22	FB_D19	$\overline{\text{FB\_BE/BWE2}}$	FB_D6	FB_D2	$\overline{\text{FB\_OE}}$	PST1	DDATA1	TMS	ADC_IN6	ADC_IN4	ADC_IN2	N
P	FB_CLK	$\overline{\text{SD\_RAS}}$	FB_D21	FB_D18	SD_DQS0	FB_D5	FB_D1	TCLK	PST0	DDATA0	$\overline{\text{TRST}}$	ADC_IN7	ADC_IN5	ADC_IN3	P

Figure 8. MCF52277 Pinout (196 MAPBGA)

## 5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5227x microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

**NOTE**

The parameters specified in this MCU document supersede any values found in the module specifications.

**5.1 Maximum Ratings****Table 7. Absolute Maximum Ratings<sup>1, 2</sup>**

Characteristic	Symbol	Value	Unit
Core Supply Voltage	$IV_{DD}$	-0.5 to +2.0	V
CMOS Pad Supply Voltage	$EV_{DD}$	-0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	$SDV_{DD}$	-0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	-0.3 to +2.0	V
Digital Input Voltage <sup>3</sup>	$V_{IN}$	-0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) <sup>3, 4, 5</sup>	$I_D$	25	mA
Operating Temperature Range (Packaged)	$T_A$ ( $T_L - T_H$ )	-40 to +85	°C
Storage Temperature Range	$T_{stg}$	-55 to +150	°C

<sup>1</sup> Functional operating conditions are given in [Section 5.4, “DC Electrical Specifications.”](#) Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

<sup>2</sup> This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $EV_{DD}$ ).

<sup>3</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>4</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $EV_{DD}$ .

<sup>5</sup> Power supply must maintain regulation within operating  $EV_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{in} > EV_{DD}$ ) is greater than  $I_D$ , the injection current may flow out of  $EV_{DD}$  and could result in external power supply going out of regulation. Insure external  $EV_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating  $EV_{DD}$  range during instantaneous and operating maximum current conditions.



## 5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	196 MAPBGA	176 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	$\theta_{JMA}$	47 <sup>1,2</sup>	TBD	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$\theta_{JMA}$	43 <sup>1,2</sup>	TBD	°C/W
Junction to board		$\theta_{JB}$	36 <sup>3</sup>	TBD	°C/W
Junction to case		$\theta_{JC}$	22 <sup>4</sup>	TBD	°C/W
Junction to top of package		$\Psi_{jt}$	6 <sup>1,5</sup>	TBD	°C/W
Maximum operating junction temperature		$T_j$	105	TBD	°C

<sup>1</sup>  $\theta_{JMA}$  and  $\Psi_{jt}$  parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of  $\theta_{JMA}$  and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the  $\Psi_{jt}$  parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

<sup>2</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>3</sup> Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>4</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

<sup>5</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature ( $T_j$ ) in °C can be obtained from:

$$T_j = T_A + (P_D \times \theta_{JMA}) \quad \text{Eqn. 1}$$

Where:

$T_A$	= Ambient Temperature, °C
$\theta_{JMA}$	= Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D$	= $P_{INT} + P_{I/O}$
$P_{INT}$	= $I_{DD} \times IV_{DD}$ , Watts - Chip Internal Power
$P_{I/O}$	= Power Dissipation on Input and Output Pins - User Determined

For most applications  $P_{I/O} < P_{INT}$  and can be ignored. An approximate relationship between  $P_D$  and  $T_j$  (if  $P_{I/O}$  is neglected) is:

$$P_D = \frac{K}{(T_j + 273^\circ\text{C})} \quad \text{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273^\circ\text{C}) + \theta_{JMA} \times P_D^2 \quad \text{Eqn. 3}$$

## Electrical Characteristics

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving Equation 1 and Equation 2 iteratively for any value of  $T_A$ .

## 5.3 ESD Protection

Table 9. ESD Protection Characteristics<sup>1,2</sup>

Characteristic	Symbol	Value	Unit
ESD Target for Human Body Model	HBM	2000	V

<sup>1</sup> All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	$IV_{DD}$	1.4	1.6	V
PLL Supply Voltage	$PLL_{V_{DD}}$	1.4	1.6	V
CMOS Pad Supply Voltage	$EV_{DD}$	3.0	3.6	V
SDRAM and FlexBus Supply Voltage	$SDV_{DD}$			V
Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V)		1.7	1.95	
DDR/Bus Pad Supply Voltage (nominal 2.5V)		2.25	2.75	
SDR/Bus Pad Supply Voltage (nominal 3.3V)		3.0	3.6	
USB Supply Voltage	$USB_{V_{DD}}$	3.0	3.6	V
CMOS Input High Voltage	$EV_{IH}$	2	$EV_{DD} + 0.3$	V
CMOS Input Low Voltage	$EV_{IL}$	$V_{SS} - 0.3$	0.8	V
CMOS Output High Voltage $I_{OH} = -5.0$ mA	$EV_{OH}$	$EV_{DD} - 0.4$	—	V
CMOS Output Low Voltage $I_{OL} = 5.0$ mA	$EV_{OL}$	—	0.4	V
SDRAM and FlexBus Input High Voltage	$SDV_{IH}$			V
Mobile DDR/Bus Input High Voltage (nominal 1.8V)		1.35	$SDV_{DD} + 0.3$	
DDR/Bus Pad Supply Voltage (nominal 2.5V)		1.7	$SDV_{DD} + 0.3$	
SDR/Bus Pad Supply Voltage (nominal 3.3V)		2	$SDV_{DD} + 0.3$	
SDRAM and FlexBus Input Low Voltage	$SDV_{IL}$			V
Mobile DDR/Bus Input High Voltage (nominal 1.8V)		$V_{SS} - 0.3$	0.45	
DDR/Bus Pad Supply Voltage (nominal 2.5V)		$V_{SS} - 0.3$	0.8	
SDR/Bus Pad Supply Voltage (nominal 3.3V)		$V_{SS} - 0.3$	0.8	

Table 10. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) $I_{OH} = -5.0$ mA for all modes	$SDV_{OH}$	1.4 2.1 2.4	— — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) $I_{OL} = 5.0$ mA for all modes	$SDV_{OL}$	— — —	0.3 0.3 0.5	V
Input Leakage Current $V_{in} = V_{DD}$ or $V_{SS}$ , Input-only pins	$I_{in}$	-1.0	1.0	$\mu$ A
Weak Internal Pull-Up Device Current, tested at $V_{IL}$ Max. <sup>1</sup>	$I_{APU}$	-10	-130	$\mu$ A
Input Capacitance <sup>2</sup> All input-only pins All input/output (three-state) pins	$C_{in}$	— —	7 7	pF

<sup>1</sup> Refer to the signals section for pins having weak internal pull-up devices.

<sup>2</sup> This parameter is characterized before qualification rather than 100% tested.

## 5.5 Oscillator and PLL Electrical Characteristics

Table 11. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range Crystal reference External reference	$f_{ref\_crystal}$	16	66.67	MHz
		$f_{ref\_ext}$	16	66.67	MHz
2	Core/system frequency CLKOUT Frequency	$f_{sys}$	TBD	166.67	MHz
		$f_{sys/2}$	TBD	83.33	MHz
3	Crystal Start-up Time <sup>1,2</sup>	$t_{cst}$	—	10	ms
4	EXTAL Input High Voltage Crystal Mode <sup>3</sup> All other modes (External, Limp)	$V_{IHEXT}$	$V_{XTAL} + 0.4$	—	V
		$V_{IHEXT}$	$E_{VDD}/2 + 0.4$	—	V
5	EXTAL Input Low Voltage Crystal Mode <sup>3</sup> All other modes (External, Limp)	$V_{ILEXT}$	—	$V_{XTAL} - 0.4$	V
		$V_{ILEXT}$	—	$E_{VDD}/2 - 0.4$	V
7	PLL Lock Time <sup>1,4</sup>	$t_{pll}$	—	50000	CLKIN
8	Duty cycle of reference <sup>1</sup>	$t_{dc}$	40	60	%
9	XTAL Current	$I_{XTAL}$	1	3	mA
10	Total on-chip stray capacitance on XTAL	$C_{S\_XTAL}$		1.5	pF
11	Total on-chip stray capacitance on EXTAL	$C_{S\_EXTAL}$		1.5	pF
12	Crystal capacitive load	$C_L$	See crystal spec		

Table 11. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min	Max	Unit
13	Discrete load capacitance for XTAL Discrete load capacitance for EXTAL	$C_{L\_XTAL}$ $C_{L\_EXTAL}$	—	$2 \times (C_L - C_{S\_XTAL} - C_{S\_EXTAL} - C_{S\_PCB})^5$	pF
14	Frequency un-LOCK Range	$f_{UL}$	-4.0	4.0	% $f_{sys}$
15	Frequency LOCK Range	$f_{LCK}$	-2.0	2.0	% $f_{sys}$
17	CLKOUT period jitter <sup>2, 3, 6</sup> measured at $f_{sys}$ max Peak-to-peak jitter (Clock edge to clock edge) Long-term jitter	$C_{jitter}$	— —	10 TBD	% $f_{sys}/2$ % $f_{sys}/2$
19	VCO frequency ( $f_{vco} = f_{ref} \times PFDR$ )	$f_{vco}$	350	540	MHz

<sup>1</sup> This parameter is guaranteed by characterization before qualification rather than 100% tested. Applies to external clock reference only.

<sup>2</sup> Proper PC board layout procedures must be followed to achieve specifications.

<sup>3</sup> This parameter is guaranteed by design rather than 100% tested.

<sup>4</sup> This specification is the PLL lock time only and does not include oscillator start-up time..

<sup>5</sup>  $C_{S\_PCB}$  is the measured PCB stray capacitance on EXTAL and XTAL.

<sup>6</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{sys}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL  $V_{DD}$ ,  $EV_{DD}$ , and  $V_{SS}$  and variation in crystal oscillator frequency increase the  $C_{jitter}$  percentage for a given interval.

## 5.6 ASP Electrical Characteristics

Table 12 lists the electrical specifications for the ASP module.

Table 12. ASP Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
ASP Analog Supply Voltage	$V_{DDA}$	3.0	3.6	V
Input Voltage Range	$V_{ADIN}$	0	$V_{DDA}$	V
Internal Reference Voltage	$V_{REF}$	TBD	700	V
Operating Current Consumption	$I_{DDA\_ON}$	TBD	700	uA
Power-down Current Consumption	$I_{DDA\_OFF}$	TBD	1	uA
Resolution	$R_{ES}$	—	12	bits
Sampling rate		—	125	KS/s
Integral Non-linearity	INL	TBD	TBD	lsb <sup>1</sup>
Differential Non-linearity	DNL	TBD	TBD	lsb <sup>1</sup>
ADC Internal Clock Frequency	$t_{AIC}$	2	8	MHz
Conversion Range	$R_{AD}$	0	$V_{DDA}$	V
Conversion Time	$t_{ADC}$	15	32	$t_{AIC}$ cycles
Sample Time	$t_{ADS}$	3	20	$t_{AIC}$ cycles

Table 12. ASP Electrical Characteristics (continued)

Characteristic	Symbol	Min	Max	Unit
Multiplexer Settling Time	$t_{AMS}$		3	$t_{AIC}$ cycles
Gain Error	GE	-4	4	lsb <sup>1</sup>
Offset Error	OE	-2	2	lsb <sup>1</sup>
Input Capacitance	$C_{AIN}$		34	pF
Input Leakage Current	$I_{ALEAK}$			uA
Input Current (Touchscreen enable)	$I_{IN\_TS\_E}$			uA

<sup>1</sup> lsb: least significant bit

## 5.6.1 Gain Calculations

The ideal mapping of input voltage to output digital sample is defined as follows:

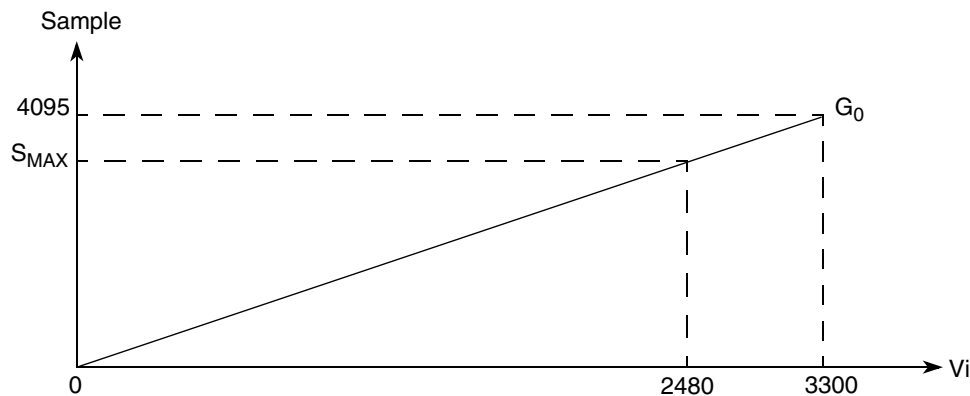


Figure 9. Gain Calculations

In general, the mapping function is:

$$S = G * V \quad \text{Eqn. 4}$$

Where V is input, S is output, and G is the slope.

$$\text{Nominal Gain } G_0 = 4095/3300 = 1.24\text{mV}^{-1} \quad \text{Eqn. 5}$$

## 5.7 External Interface Timing Specifications

### 5.7.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

## Electrical Characteristics

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB\_CLK. The FB\_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the Flexbus output clock, FB\_CLK. All other timing relationships can be derived from these values.

**Table 13. FlexBus AC Timing Specifications**

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		—	83.33	MHz	$f_{sys/2}$
FB1	Clock Period (FB_CLK)	$t_{FBCK}$	12.0	—	ns	$t_{cyc}$
FB2	Address, Data, and Control Output Valid (FB_A[23:0], FB_D[31:0], FB_CS[5:0], FB_R/W, FB_TS, FB_BE/BWE[3:0] and FB_OE)	$t_{FBCHDCV}$	—	7.0	ns	1
FB3	Address, Data, and Control Output Hold (FB_A[23:0], FB_D[31:0], FB_CS[5:0], FB_R/W, FB_TS, FB_BE/BWE[3:0], and FB_OE)	$t_{FBCHDCI}$	1	—	ns	1, 2
FB4	Data Input Setup	$t_{DVFBCH}$	3.5	—	ns	
FB5	Data Input Hold	$t_{DIFBCH}$	0	—	ns	
FB6	Transfer Acknowledge ( $\overline{TA}$ ) Input Setup	$t_{CVFBCH}$	4	—	ns	
FB7	Transfer Acknowledge ( $\overline{TA}$ ) Input Hold	$t_{CIFBCH}$	0	—	ns	

<sup>1</sup> Timing for chip selects only applies to the FB\_CS[5:0] signals. Please see [Section 5.7.2.2, “DDR SDRAM AC Timing Specifications,”](#) for SD\_CS[3:0] timing.

<sup>2</sup> The FlexBus supports programming an extension of the address hold. Please consult the device reference manual for more information.

### NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

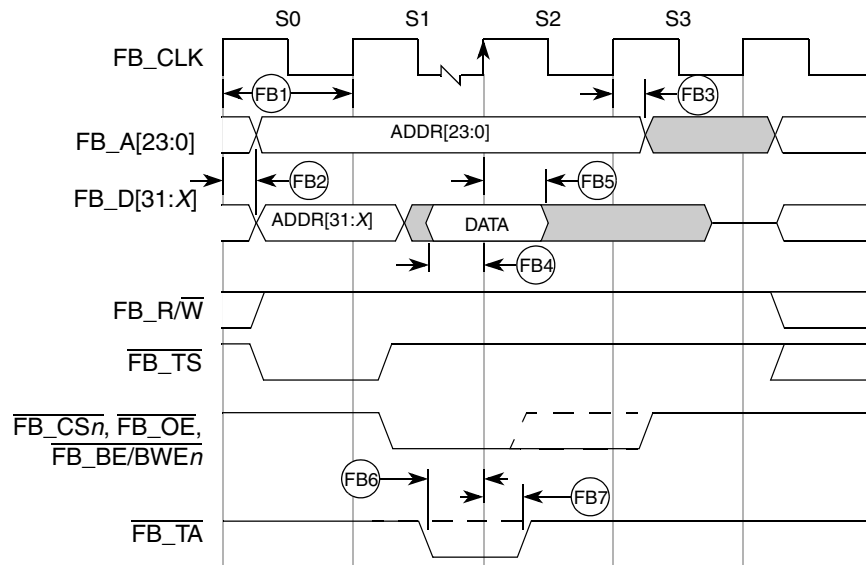


Figure 10. FlexBus Read Timing

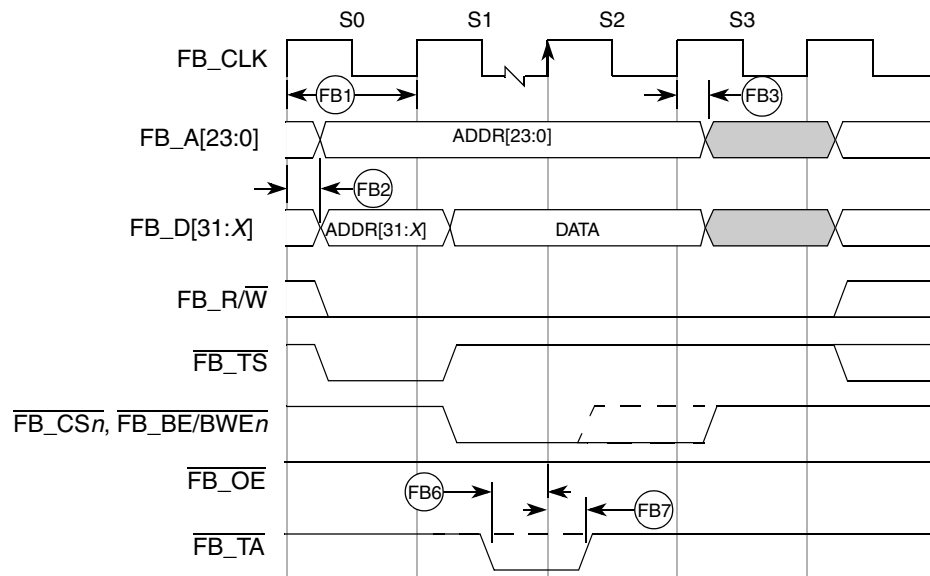


Figure 11. Flexbus Write Timing

## 5.7.2 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports either standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

### 5.7.2.1 SDR SDRAM AC Timing Specifications

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD\_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must still be supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD\_SDR\_DQS during

## Electrical Characteristics

read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD\_SDR\_DQS signal and its usage.

**Table 14. SDR Timing Specifications**

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		TBD	83.33	MHz	1
SD1	Clock Period	$t_{SDCK}$	12.0	TBD	ns	2
SD2	Pulse Width High	$t_{SDCKH}$	0.45	0.55	SD_CLK	3
SD3	Pulse Width Low	$t_{SDCKL}$	0.45	0.55	SD_CLK	3
SD4	Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_BA, SD_CS[1:0] - Output Valid	$t_{SDCHACV}$	—	$0.5 \times SD\_CLK + 1.0$	ns	
SD5	Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_BA, SD_CS[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	
SD6	SD_SDR_DQS Output Valid	$t_{DQSOV}$	—	Self timed	ns	4
SD7	SD_DQS[3:2] input setup relative to SD_CLK	$t_{DQVSDCH}$	$0.25 \times SD\_CLK$	$0.40 \times SD\_CLK$	ns	5
SD8	SD_DQS[3:2] input hold relative to SD_CLK	$t_{DQISDCH}$	Does not apply. $0.5 \times SD\_CLK$ fixed width.			6
SD9	Data (D[31:0]) Input Setup relative to SD_CLK (reference only)	$t_{DVS DCH}$	$0.25 \times SD\_CLK$	—	ns	7
SD10	Data Input Hold relative to SD_CLK (reference only)	$t_{DIS DCH}$	1.0	—	ns	
SD11	Data (D[31:0]) and Data Mask(SD_DQM[3:0]) Output Valid	$t_{SDCHDMV}$	—	$0.5 \times SD\_CLK + 2$	ns	
SD12	Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Hold	$t_{SDCHDMI}$	1.5	—	ns	

<sup>1</sup> The device supports same frequency of operation for both FlexBus and SDRAM clock operates as that of the internal bus clock. Please see the PLL chapter of the device reference manual for more information on setting the SDRAM clock rate.

<sup>2</sup> SD\_CLK is one SDRAM clock in ns.

<sup>3</sup> Pulse width high plus pulse width low cannot exceed min and max clock period.

<sup>4</sup> SD\_SDR\_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD\_SDR\_DQS will only pulse during a read cycle and one pulse will occur for each data beat.

<sup>5</sup> SD\_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SD\_DQS will only pulse during a read cycle and one pulse will occur for each data beat.

<sup>6</sup> The SD\_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

<sup>7</sup> Since a read cycle in SDR mode still uses the DQS circuit within the device, it is critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens will result in successful SDR reads. The input setup spec is provided as guidance.



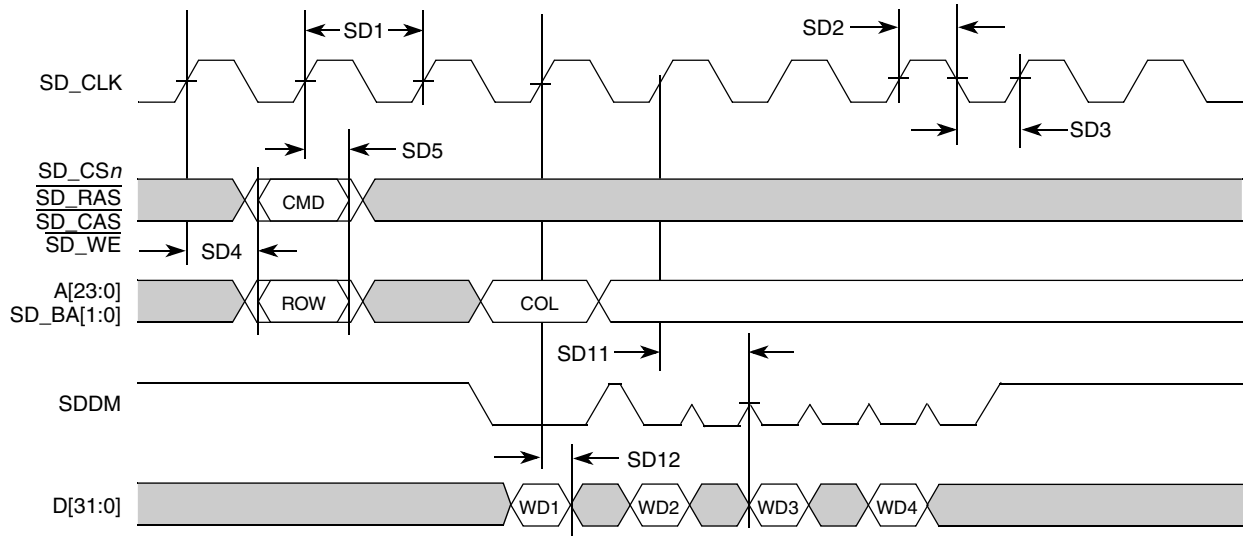


Figure 12. SDR Write Timing

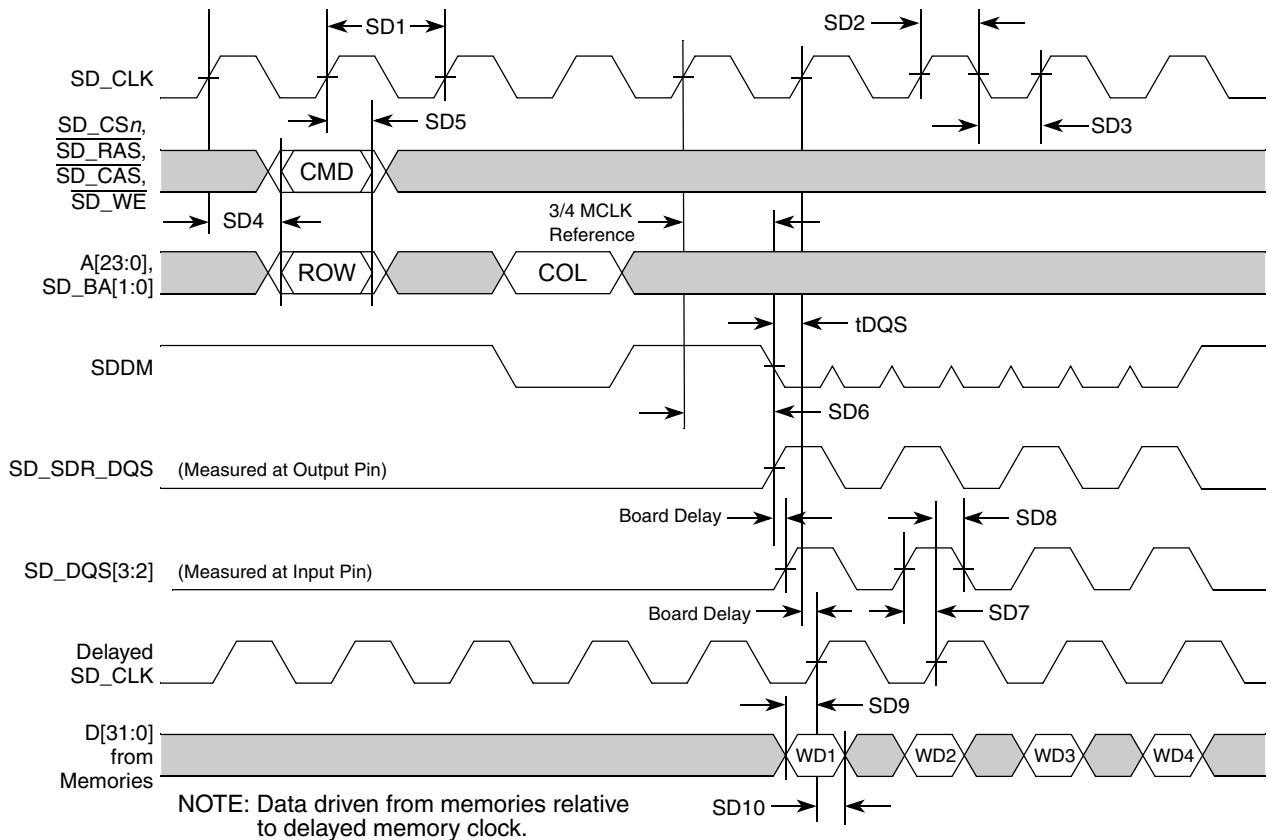


Figure 13. SDR Read Timing

### 5.7.2.2 DDR SDRAM AC Timing Specifications

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

Table 15. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation	$t_{DDCK}$	TBD	83.33	MHz	1
DD1	Clock Period	$t_{DDSK}$	12.0	TBD	ns	2
DD2	Pulse Width High	$t_{DDCKH}$	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	$t_{DDCKL}$	0.45	0.55	SD_CLK	3
DD4	Address, $\overline{SD\_CKE}$ , $\overline{SD\_CAS}$ , $\overline{SD\_RAS}$ , $\overline{SD\_WE}$ , $\overline{SD\_CS}[1:0]$ - Output Valid	$t_{SDCHACV}$	—	$0.5 \times SD\_CLK + 1.0$	ns	4
DD5	Address, $\overline{SD\_CKE}$ , $\overline{SD\_CAS}$ , $\overline{SD\_RAS}$ , $\overline{SD\_WE}$ , $\overline{SD\_CS}[1:0]$ - Output Hold	$t_{SDCHACI}$	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	$t_{CMDVDQ}$	—	1.25	SD_CLK	
DD7	Data and Data Mask Output Setup (DQ→DQS) Relative to DQS (DDR Write Mode)	$t_{DQDMV}$	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS→DQ) Relative to DQS (DDR Write Mode)	$t_{DQDMI}$	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	$t_{DQDQ}$	—	1	ns	8
DD10	Input Data Hold Relative to DQS	$t_{DQDQ}$	$0.25 \times SD\_CLK + 0.5ns$	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQSDCH}$	0.5	—	ns	

- <sup>1</sup> The frequency of operation is either 2x or 4x the FB\_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.
- <sup>2</sup> SD\_CLK is one SDRAM clock in ns.
- <sup>3</sup> Pulse-width high plus pulse-width low cannot exceed minimum or maximum clock period.
- <sup>4</sup> Command output valid should be one-half the memory bus clock (SD\_CLK) plus some minor adjustments for process, temperature, and voltage variations.
- <sup>5</sup> This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory will be in violation. MEM\_DATA[31:24] is relative to MEM\_DQS[3], MEM\_DATA[23:16] is relative to MEM\_DQS[2], MEM\_DATA[15:8] is relative to MEM\_DQS[1], and MEM\_DATA[7:0] is relative MEM\_DQS[0].
- <sup>6</sup> The first data beat will be valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats will be valid for each subsequent DQS edge.
- <sup>7</sup> This specification relates to the required hold time of today's DDR memories. MEM\_DATA[31:24] is relative to MEM\_DQS[3], MEM\_DATA[23:16] is relative to MEM\_DQS[2], MEM\_DATA[15:8] is relative to MEM\_DQS[1], and MEM\_DATA[7:0] is relative MEM\_DQS[0].
- <sup>8</sup> Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system-level board skew (due to routing or other factors).
- <sup>9</sup> Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

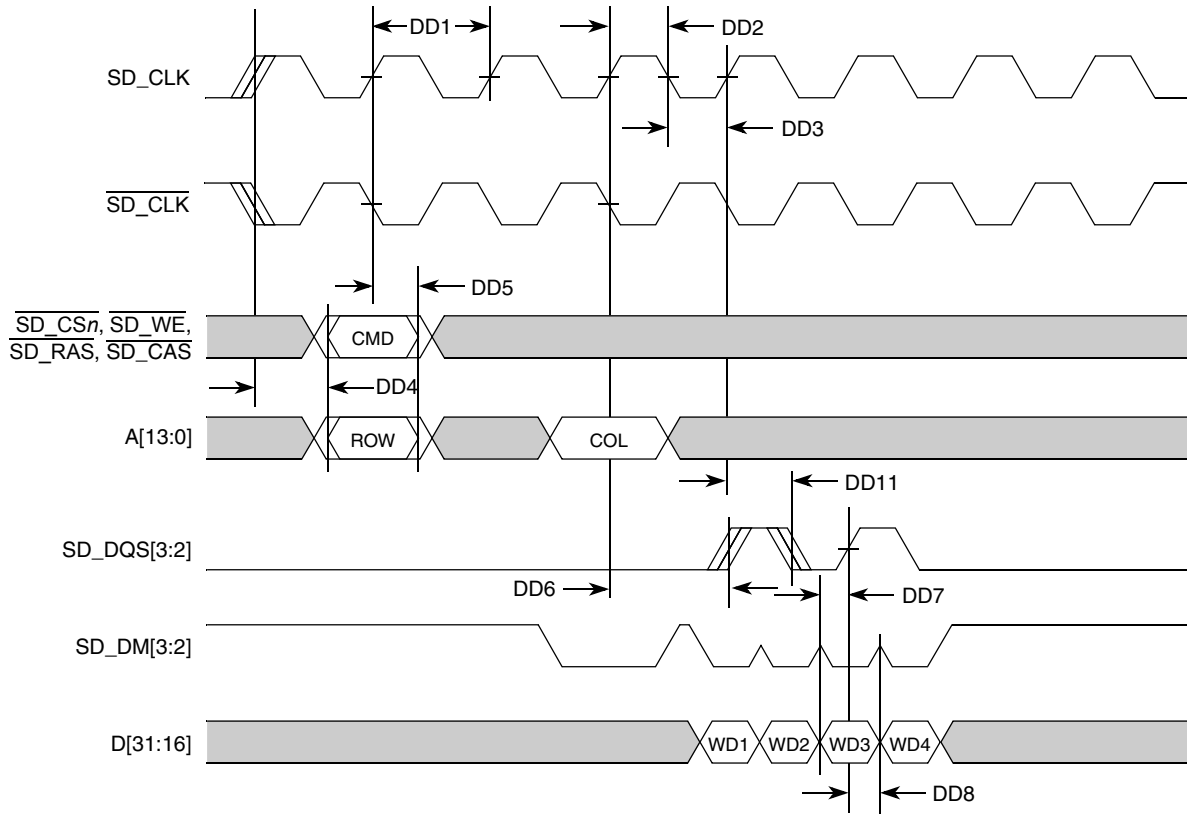


Figure 14. DDR Write Timing

## Electrical Characteristics

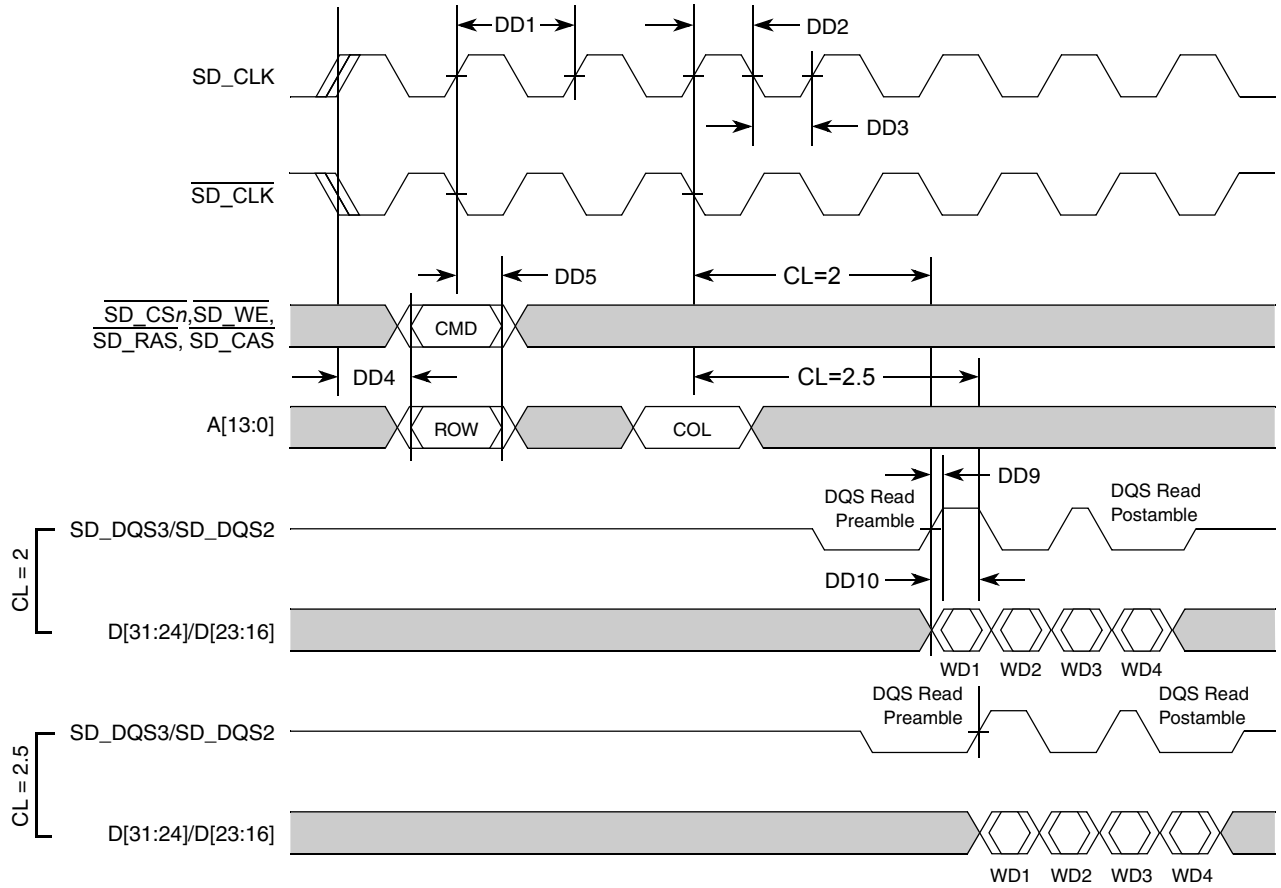


Figure 15. DDR Read Timing

Table 16. DDR Clock Crossover Specifications

Symbol	Characteristic	Min	Max	Unit
$V_{MP}$	Clock output mid-point voltage	1.05	1.45	V
$V_{OUT}$	Clock output voltage level	-0.3	$SD\_VDD + 0.3$	V
$V_{ID}$	Clock output differential voltage (peak to peak swing)	0.7	$SD\_VDD + 0.6$	V
$V_{IX}$	Clock crossing point voltage <sup>1</sup>	1.05	1.45	V

<sup>1</sup> The clock crossover voltage is only guaranteed when using the highest drive strength option for the SDCLK[1:0] and SDCLK[1:0] signals.

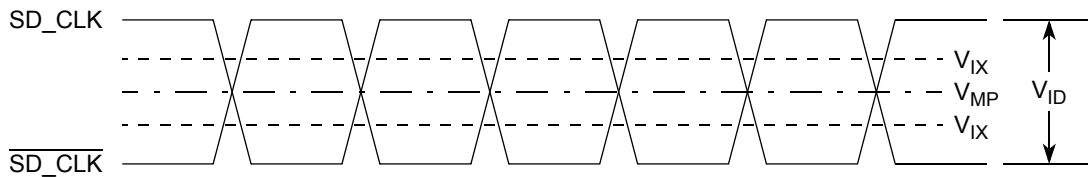


Figure 16. SD\_CLK and  $\overline{SD\_CLK}$  Crossover Timing

## 5.8 General Purpose I/O Timing

Table 17. GPIO Timing<sup>1</sup>

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	$t_{CHPOV}$	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	$t_{CHPOI}$	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	$t_{PVCH}$	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	$t_{CHPI}$	1.5	—	ns

<sup>1</sup> These general purpose specifications apply to the following signals:  $\overline{IRQn}$ , all UART signals, FlexCAN signals, PWM signals,  $\overline{DACKn}$  and  $\overline{DREQn}$ , and all signals configured as GPIO.

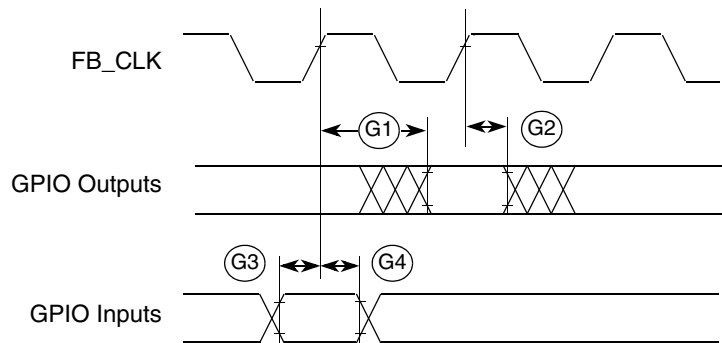


Figure 17. GPIO Timing

## 5.9 Reset and Configuration Override Timing

Table 18. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RESET}$ Input valid to FB_CLK High	$t_{RVCH}$	9	—	ns
R2	FB_CLK High to $\overline{RESET}$ Input invalid	$t_{CHRI}$	1.5	—	ns
R3	$\overline{RESET}$ Input valid Time <sup>1</sup>	$t_{RIVT}$	5	—	$t_{CYC}$
R4	FB_CLK High to $\overline{RSTOUT}$ Valid	$t_{CHROV}$	—	10	ns
R5	$\overline{RSTOUT}$ valid to Config. Overrides valid	$t_{ROVCV}$	0	—	ns
R6	Configuration Override Setup Time to $\overline{RSTOUT}$ invalid	$t_{COS}$	20	—	$t_{CYC}$
R7	Configuration Override Hold Time after $\overline{RSTOUT}$ invalid	$t_{COH}$	0	—	ns
R8	$\overline{RSTOUT}$ invalid to Configuration Override High Impedance	$t_{ROICZ}$	—	1	$t_{CYC}$

<sup>1</sup> During low power STOP, the synchronizers for the  $\overline{RESET}$  input are bypassed and  $\overline{RESET}$  is asserted asynchronously to the system. Thus,  $\overline{RESET}$  must be held a minimum of 100 ns.

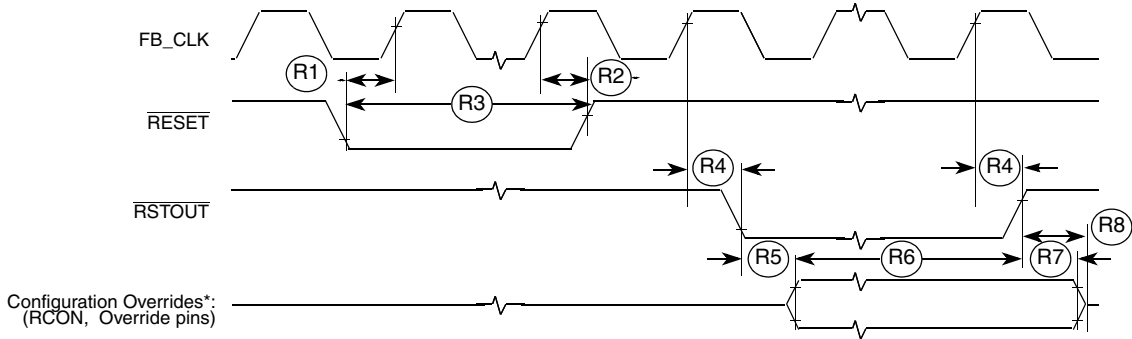


Figure 18.  $\overline{\text{RESET}}$  and Configuration Override Timing

**NOTE**

Refer to the CCM chapter of the *MCF52277 Reference Manual* for more information.

### 5.10 LCD Controller Timing Specifications

This sections lists the timing specifications for the LCD Controller.

Table 19. LCD\_LSCLK Timing

Num	Characteristic	Min	Max	Unit
T1	LCD_LSCLK Period	25	2000	ns
T2	Pixel data setup time	11	—	ns
T3	Pixel data up time	11	—	ns

**Note:** The pixel clock is equal to  $\text{LCD\_LSCLK} / (\text{PCD} + 1)$ . When it is in CSTN, TFT, or monochrome mode with bus width = 1, LCD\_LSCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, LCD\_LSCLK is equal to the pixel clock divided by bus width. The polarity of LCD\_LSCLK and LCD\_D signals can also be programmed.

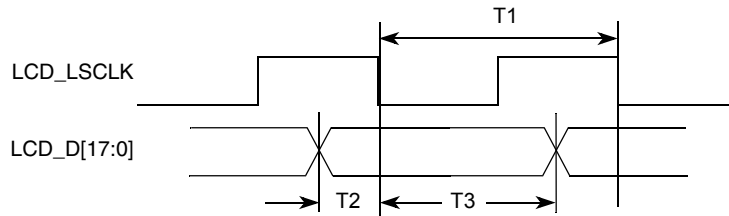


Figure 19. LCD\_LSCLK to LCD\_D[17:0] timing diagram

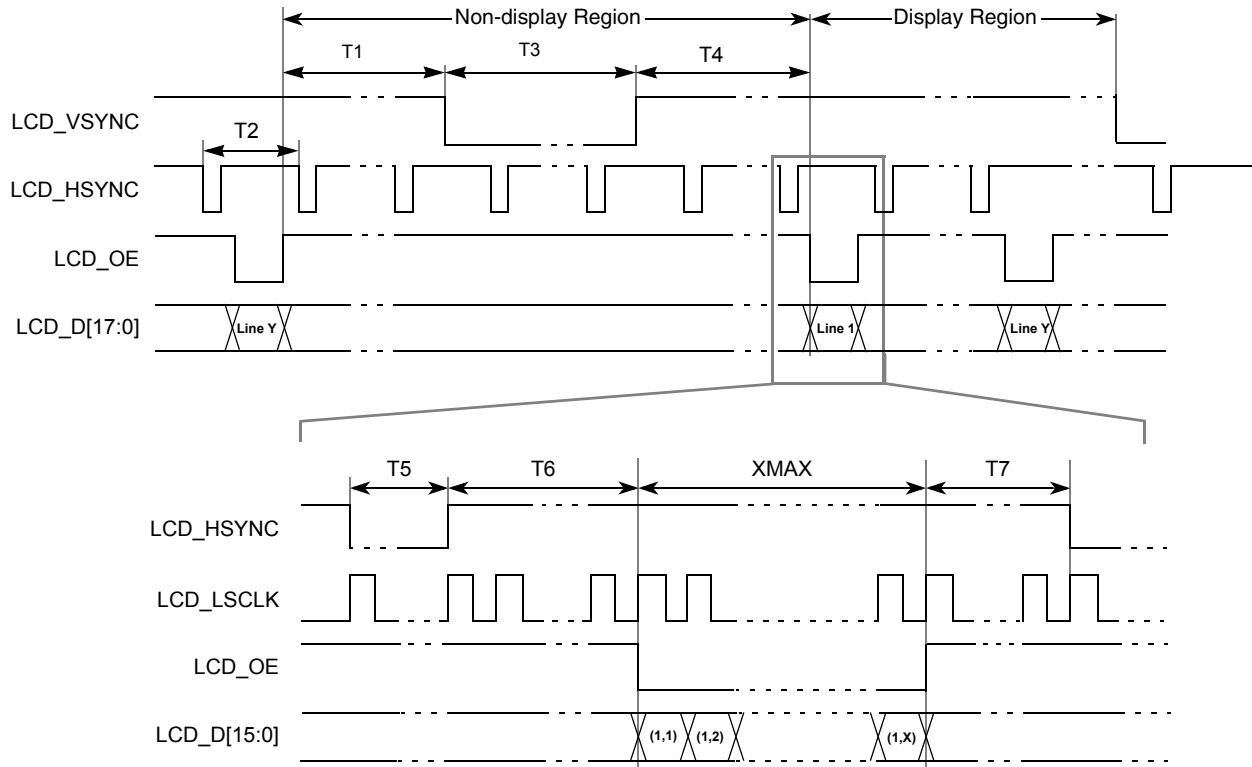


Figure 20. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Table 20. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Num	Characteristic	Min	Value	Unit
T1	End of LCD_OE to beginning of LCD_VSYNC	$T5 + T6 + T7 - 1$	$(VWAIT1 \times T2) + T5 + T6 + T7 - 1$	Ts
T2	LCD_VSYNC pulse width	T2	$VWIDTH \times T2$	Ts
T3	End of LCD_VSYNC to beginning of LCD_OE	1	$(VWAIT2 \times T2) + 1$	Ts
T4	LCD_HSYNC period	—	$XMAX + T5 + T6 + T7$	Ts
T5	LCD_HSYNC pulse width	1	$HWIDTH + 1$	Ts
T6	End of LCD_HSYNC to beginning to LCD_OE	3	$HWAIT2 + 3$	Ts
T7	End of LCD_OE to beginning of LCD_HSYNC	1	$HWAIT1 + 1$	Ts

**Note:** Ts is the LCD\_LSCLK period. LCD\_VSYNC, LCD\_HSYNC, and LCD\_OE can be programmed as active high or active low. In Figure 20, all 3 signals are active low. LCD\_LSCLK can be programmed to be deactivated during the LCD\_VSYNC pulse or the LCD\_OE deasserted period. In Figure 20, LCD\_LSCLK is always active.

**Note:** XMAX is defined in number of pixels in one line.

## Electrical Characteristics

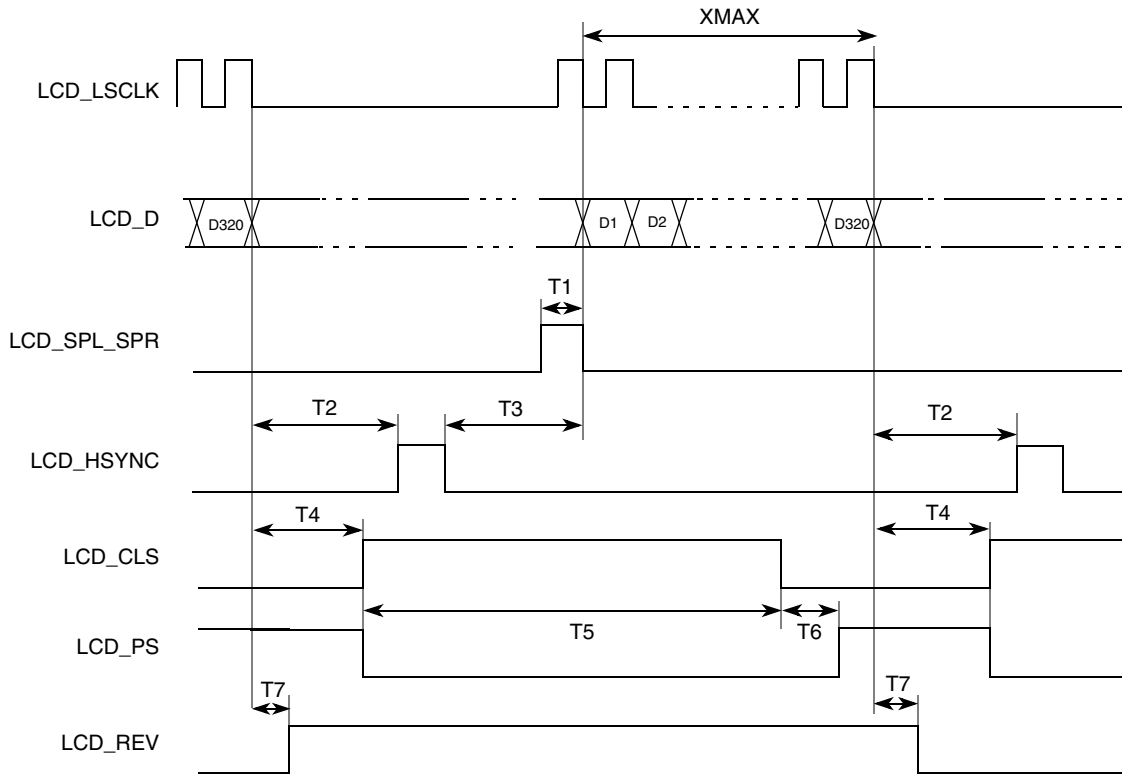


Figure 21. Sharp TFT Panel Timing

Table 21. Sharp TFT Panel Timing

Num	Characteristic	Min	Value	Unit
T1	LCD_SPL/LCD_SPR pulse width	—	1	Ts
T2	End of LCD_D of line to beginning of LCD_HSYNC	1	HWAIT1+1	Ts
T3	End of LCD_HSYNC to beginning of LCD_D of line	4	HWAIT2 + 4	Ts
T4	LCD_CLS rise delay from end of LCD_D of line	3	CLS_RISE_DELAY+1	Ts
T5	LCD_CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	LCD_PS rise delay from LCD_CLS negation	0	PS_RISE_DELAY	Ts
T7	LCD_REV toggle delay from last LCD_D of line	1	REV_TOGGLE_DELAY+1	Ts

**Note:** Falling of LCD\_SPL/LCD\_SPR aligns with first LCD\_D of line.

**Note:** Falling of LCD\_PS aligns with rising edge of LCD\_CLS.

**Note:** LCD\_REV toggles in every LCD\_HSYN period.



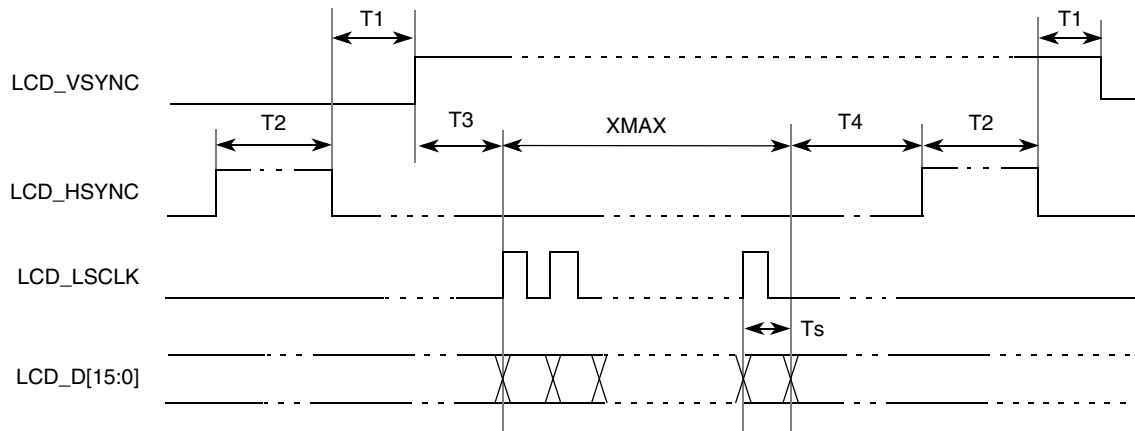


Figure 22. Non-TFT Mode Panel Timing

Table 22. Non-TFT Mode Panel Timing

Num	Characteristic	Min	Value	Unit
T1	LCD_HSYNC to LCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	LCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	LCD_VSYNC to LCD_LSCLK	—	$0 \leq T3 \leq Ts$	—
T4	LCD_LSCLK to LCD_HSYNC	1	HWAIT1 + 1	Tpix

**Note:** Ts is the LCD\_LSCLK period while Tpix is the pixel clock period. LCD\_VSYNC, LCD\_HSYNC, and LCD\_LSCLK can be programmed as active high or active low. In Figure 22, all these 3 signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

## 5.11 USB On-The-Go Specifications

The MCF5227x device is compliant with industry standard USB 2.0 specification.

Table 23. USB On-Chip Transceiver DC Characteristics

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Input High	Driven	$V_{IH}$	2.0	—	—	V
Input Low		$V_{IL}$	—	—	0.8	V
Input Differential	(DP – DM)	$V_{ID}$	200	—	00	mV
Differential Common Mode Range		$V_{CM}$	0.8	—	2.5	V
Single Ended Receive Threshold		$V_{SETHR}$	0.8	—	2.0	V
Single Ended Receive Hysteresis		$V_{SEHYS}$	—	400	—	mV
Output High	Driven	$V_{OH}$	0.0	—	300	mV
Output Low	Driven	$V_{OL}$	2.8	—	2.0	V
Differential Output Crossover	DP = DM	$V_{CRS}$	1.3	—	2.0	V

**Table 23. USB On-Chip Transceiver DC Characteristics (continued)**

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
P side Impedance	Driven	$Z_P$	6.25	8.25	11.25	$\Omega$
M side Impedance	Driven	$Z_M$	6.25	8.25	11.25	$\Omega$
Impedance Matching P/M		$Z_{\text{Matching}}$	—	0.17	0.23	$\Omega$
Pulldown Resistance <sup>1</sup>		$R_{PD}$	30k	50k	70k	$\Omega$

<sup>1</sup> The pulldown resistors are included to provide a method to keep DP and DM signals in a known quiescent state if desired when the USB port is not being used or when the USB cable is not connected. These on-chip resistors should not be used to provide the 15-k $\Omega$  host-mode pulldowns called for in Chapter 7 of the USB Specification, Rev. 1.1 or Rev. 2.0.

**Table 24. USB On-Chip Transceiver Full Speed AC Characteristics**

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Rise Time	10–90%	$t_{LH}$	7	11	17.5	ns
Fall Time	90–10%	$t_{HL}$	7	11	17.5	ns
Rise/Fall Matching	—	$\frac{t_{LH}}{t_{HL}}$ Matching	20	40	60	ps
Rise/Fall Matching, DP and DM	—	$\frac{t_{LH}}{t_{HL}}$ Pad-to-Pad	330	360	640	ps
Time Skew Between DP and DM	—	$t_{SKE}$	100	140	210	ps

**Table 25. USB On-Chip Transceiver Low Speed AC Characteristics**

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Rise Time	10–90%	$t_{LH}$	75	—	300	ns
Fall Time	90–10%	$t_{HL}$	75	—	300	ns
Rise/Fall Matching	$\frac{t_{LH}}{t_{HL}}$	$\frac{t_{LH}}{t_{HL}}$ Matching	80	—	125	%

## 5.12 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI\_TCR[TCKP] = 0, SSI\_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI\_TCR[TFSI] = 0, SSI\_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI\_BCLK) and/or the frame sync (SSI\_FS) shown in the figures below.

**Table 26. SSI Timing—Master Modes<sup>1</sup>**

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S1	SSI_MCLK cycle time	$t_{MCLK}$	$4 \times t_{SYS}$	—	ns	<sup>2</sup>
S2	SSI_MCLK pulse width high / low		45%	55%	$t_{MCLK}$	
S3	SSI_BCLK cycle time	$t_{BCLK}$	$4 \times t_{SYS}$	—	ns	<sup>3</sup>
S4	SSI_BCLK pulse width		45%	55%	$t_{BCLK}$	

Table 26. SSI Timing—Master Modes<sup>1</sup> (continued)

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S5	SSI_BCLK to SSI_FS output valid		—	10	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	10	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedance		0	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

<sup>1</sup> All timings specified with a capacitive load of 25pF.

<sup>2</sup> SSI\_MCLK can be generated from SSI\_CLKIN or a divided version of the internal system clock (SYSCLK).

<sup>3</sup> SSI\_BCLK can be derived from SSI\_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI\_CLKIN input is used, the programmable dividers must be set to ensure that SSI\_BCLK does not exceed  $4 \times f_{\text{SYS}}$ .

Table 27. SSI Timing—Slave Modes<sup>1</sup>

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S11	SSI_BCLK cycle time	$t_{\text{BCLK}}$	$4 \times t_{\text{SYS}}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	$t_{\text{BCLK}}$	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	10	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedance		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

<sup>1</sup> All timings specified with a capacitive load of 25 pF.

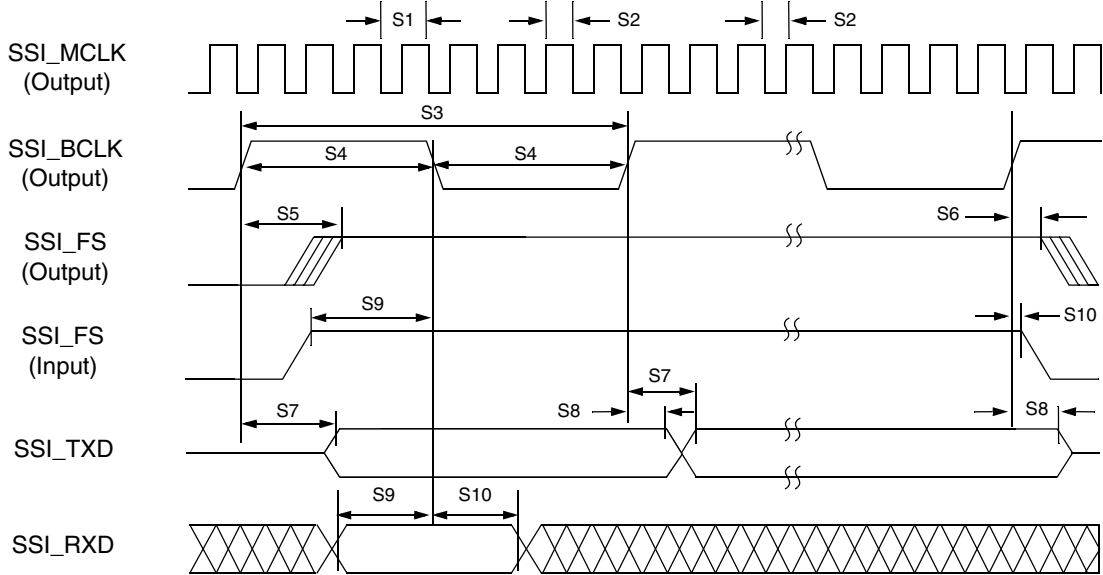


Figure 23. SSI Timing—Master Modes

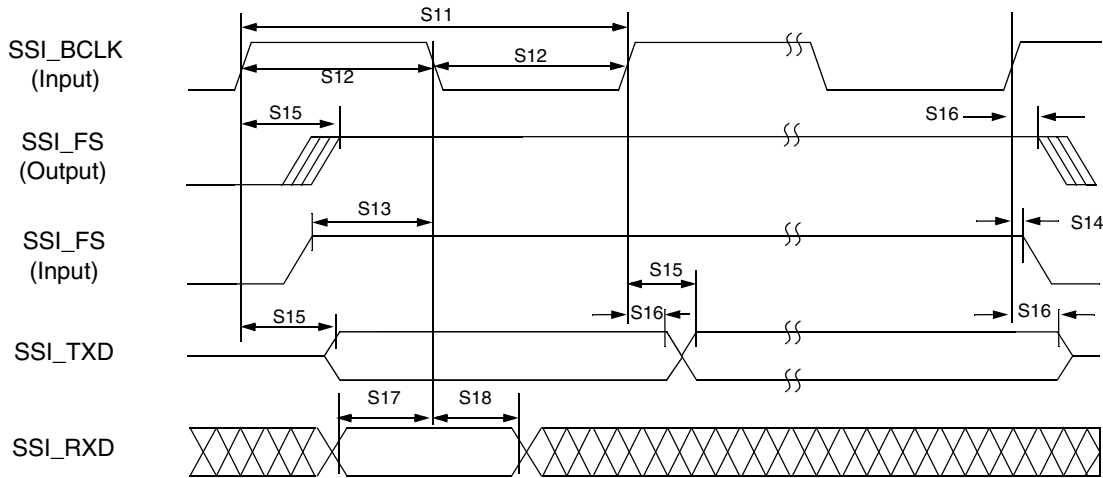


Figure 24. SSI Timing—Slave Modes

### 5.13 I<sup>2</sup>C Timing Specifications

Table 28 lists specifications for the I<sup>2</sup>C input timing parameters shown in Figure 25.

Table 28. I<sup>2</sup>C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Unit
I1	Start condition hold time	2	—	t <sub>cyc</sub>
I2	Clock low period	8	—	t <sub>cyc</sub>
I3	I <sup>2</sup> C_SCL/I <sup>2</sup> C_SDA rise time (V <sub>IL</sub> = 0.5 V to V <sub>IH</sub> = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

**Table 28. I<sup>2</sup>C Input Timing Specifications between SCL and SDA (continued)**

Num	Characteristic	Min	Max	Unit
I5	I2C_SCL/I2C_SDA fall time ( $V_{IH} = 2.4\text{ V}$ to $V_{IL} = 0.5\text{ V}$ )	—	1	ms
I6	Clock high time	4	—	$t_{cyc}$
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	$t_{cyc}$
I9	Stop condition setup time	2	—	$t_{cyc}$

Table 29 lists specifications for the I<sup>2</sup>C output timing parameters shown in Figure 25.

**Table 29. I<sup>2</sup>C Output Timing Specifications between SCL and SDA**

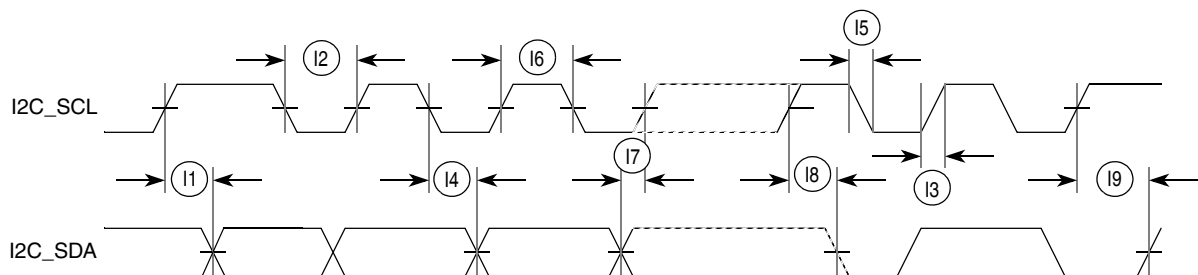
Num	Characteristic	Min	Max	Unit
I1 <sup>1</sup>	Start condition hold time	6	—	$t_{cyc}$
I2 <sup>1</sup>	Clock low period	10	—	$t_{cyc}$
I3 <sup>2</sup>	I2C_SCL/I2C_SDA rise time ( $V_{IL} = 0.5\text{ V}$ to $V_{IH} = 2.4\text{ V}$ )	—	—	$\mu\text{s}$
I4 <sup>1</sup>	Data hold time	7	—	$t_{cyc}$
I5 <sup>3</sup>	I2C_SCL/I2C_SDA fall time ( $V_{IH} = 2.4\text{ V}$ to $V_{IL} = 0.5\text{ V}$ )	—	3	ns
I6 <sup>1</sup>	Clock high time	10	—	$t_{cyc}$
I7 <sup>1</sup>	Data setup time	2	—	$t_{cyc}$
I8 <sup>1</sup>	Start condition setup time (for repeated start condition only)	20	—	$t_{cyc}$
I9 <sup>1</sup>	Stop condition setup time	10	—	$t_{cyc}$

<sup>1</sup> Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 29. The I<sup>2</sup>C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 29 are minimum values.

<sup>2</sup> Because I2C\_SCL and I2C\_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C\_SCL or I2C\_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

<sup>3</sup> Specified at a nominal 50-pF load.

Figure 25 shows timing for the values in Table 29 and Table 28.

**Figure 25. I<sup>2</sup>C Input/Output Timings**

## 5.14 DMA Timer Timing Specifications

Table 30 lists timer module AC timings.

**Table 30. Timer Module AC Timing Specifications**

Num	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t <sub>CYC</sub>
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t <sub>CYC</sub>

## 5.15 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with both master and slave operations. Many of the transfer attributes are programmable. Table 31 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF52277 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 31. DSPI Module AC Timing Specifications<sup>1</sup>**

Num	Characteristic	Symbol	Min	Max	Unit	Notes
DS1	DSPI_SCK Cycle Time	t <sub>SCK</sub>	4 × t <sub>SYS</sub>	—	ns	<sup>2</sup>
DS2	DSPI_SCK Duty Cycle	—	(t <sub>sck</sub> ÷ 2) – 2.0	(t <sub>sck</sub> ÷ 2) + 2.0	ns	
<b>Master Mode</b>						
DS3	DSPI_PCS <sub>n</sub> to DSPI_SCK delay	t <sub>CSC</sub>	(2 × t <sub>SYS</sub> ) – 2.0	—	ns	<sup>3</sup>
DS4	DSPI_SCK to DSPI_PCS <sub>n</sub> delay	t <sub>ASC</sub>	(2 × t <sub>SYS</sub> ) – 3.0	—	ns	<sup>4</sup>
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—	–5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	9	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
<b>Slave Mode</b>						
DS9	DSPI_SCK to DSPI_SOUT valid	—	—	4	ns	
DS10	DSPI_SCK to DSPI_SOUT invalid	—	0	—	ns	
DS11	DSPI_SIN to DSPI_SCK input setup	—	2	—	ns	
DS12	DSPI_SCK to DSPI_SIN input hold	—	7	—	ns	
DS13	DSPI_SS active to DSPI_SOUT driven	—	—	20	ns	
DS14	DSPI_SS inactive to DSPI_SOUT not driven	—	—	18	ns	

<sup>1</sup> Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTAR<sub>n</sub>[CPHA] = 0. Data is sampled on the DSPI\_SIN pin on the odd-numbered DSPI\_SCK edges and driven on the DSPI\_SOUT pin on even-numbered DSPI edges.

<sup>2</sup> When in master mode, the baud rate is programmable in DCTAR<sub>n</sub>[PBR] and DCTAR<sub>n</sub>[BR].

<sup>3</sup> The DSPI\_PCS<sub>n</sub> to DSPI\_SCK delay is programmable in DCTAR<sub>n</sub>[PCSSCK] and DCTAR<sub>n</sub>[CSSCK].

<sup>4</sup> The DSPI\_SCK to DSPI\_PCS<sub>n</sub> delay is programmable in DCTAR<sub>n</sub>[PASC] and DCTAR<sub>n</sub>[ASC].

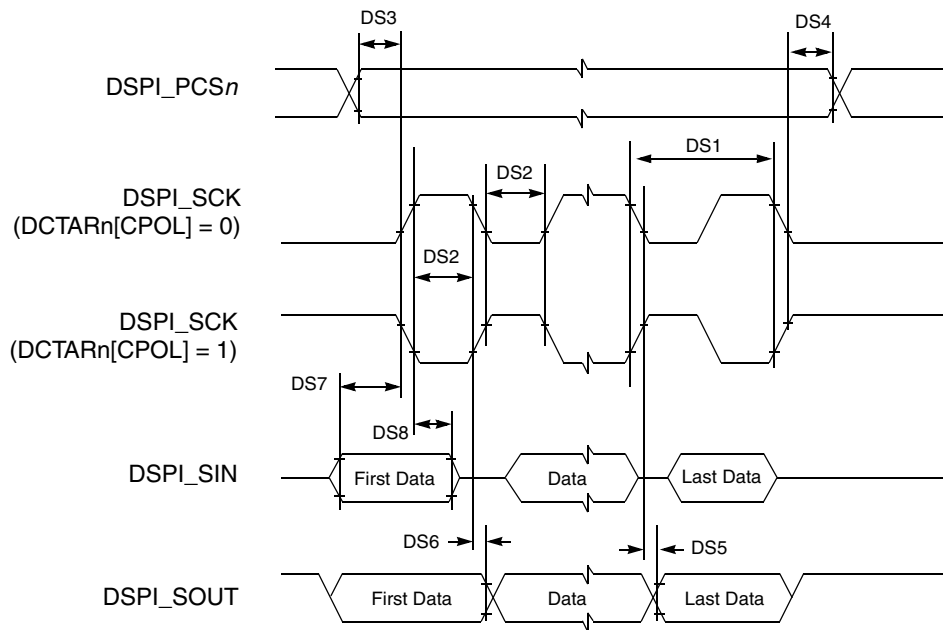


Figure 26. DSPI Classic SPI Timing—Master Mode

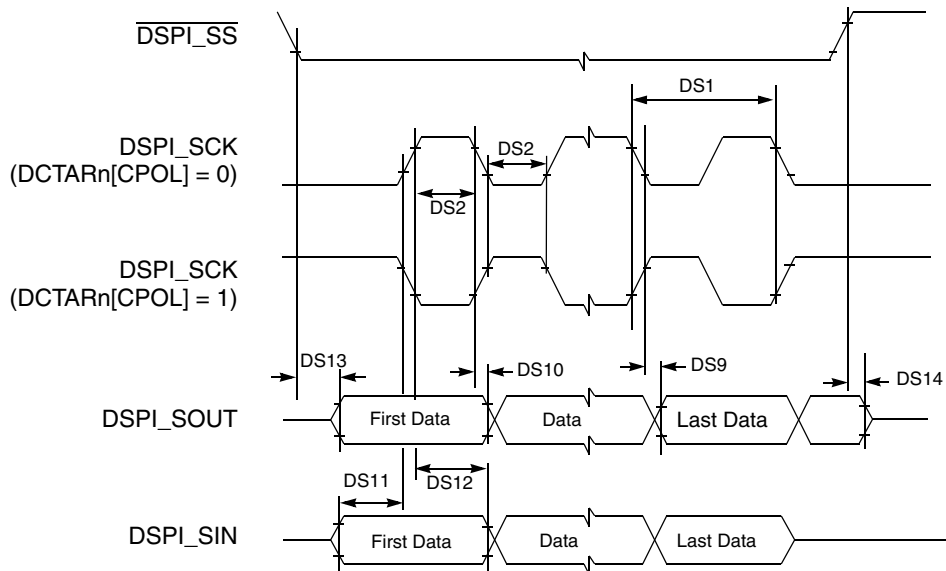


Figure 27. DSPI Classic SPI Timing—Slave Mode

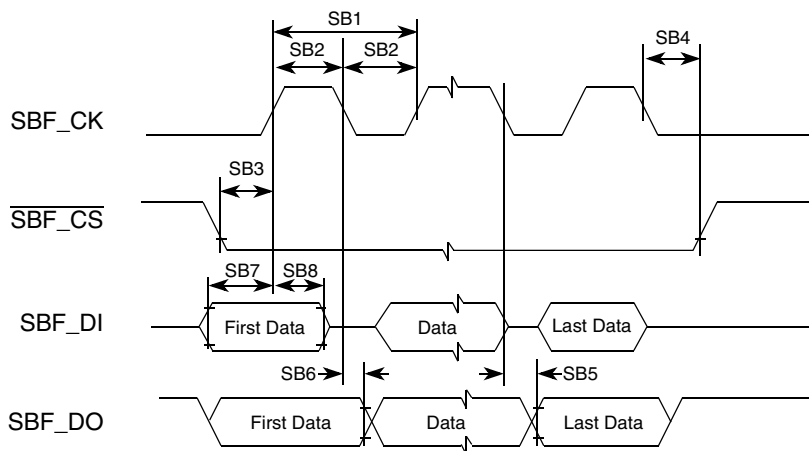
## 5.16 SBF Timing Specifications

The Serial Boot Facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. [Table 32](#) provides the AC timing specifications for the SBF.

**Table 32. SBF AC Timing Specifications**

Num	Characteristic	Symbol	Min	Max	Unit	Notes
SB1	SBF_CK Cycle Time	$t_{SBFCK}$	30	—	ns	1
SB2	SBF_CK High/Low Time	—	30%	—	$t_{SBFCK}$	
SB3	$\overline{SBF\_CS}$ to SBF_CK delay	—	$t_{SBFCK} - 2.0$	—	ns	
SB4	SBF_CK to $\overline{SBF\_CS}$ delay	—	$t_{SBFCK} - 2.0$	—	ns	
SB5	SBF_CK to SBF_DO valid	—	—	12	ns	
SB6	SBF_CK to SBF_DO invalid	—	0	—	ns	
SB7	SBF_DI to SBF_SCK input setup	—	6	—	ns	
SB8	SBF_CK to SBF_DI input hold	—	0	—	ns	

<sup>1</sup> At reset, the SBF\_CK cycle time is  $t_{REF} \times 67$ . The first byte of data read from the serial memory contains a divider value that is used to set the SBF\_CK cycle time for the duration of the serial boot process.



**Figure 28. SBF Timing**

## 5.17 JTAG and Boundary Scan Timing Specifications

**Table 33. JTAG and Boundary Scan Timing**

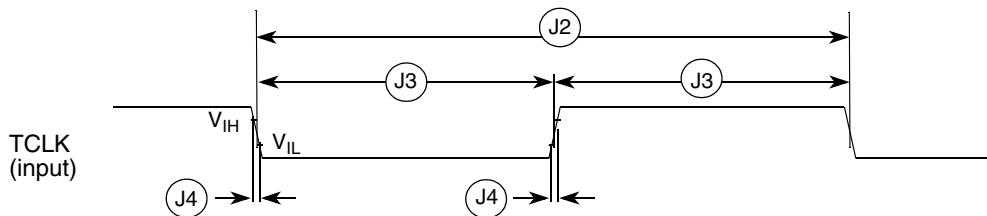
Num	Characteristic <sup>1</sup>	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	$f_{JCYC}$	DC	1/4	$f_{sys}/2$
J2	TCLK Cycle Period	$t_{JCYC}$	4	—	$t_{CYC}$
J3	TCLK Clock Pulse Width	$t_{JCW}$	26	—	ns
J4	TCLK Rise and Fall Times	$t_{JCRF}$	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	$t_{BSDST}$	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	$t_{BSDHT}$	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	$t_{BSDV}$	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	$t_{BSDZ}$	0	33	ns



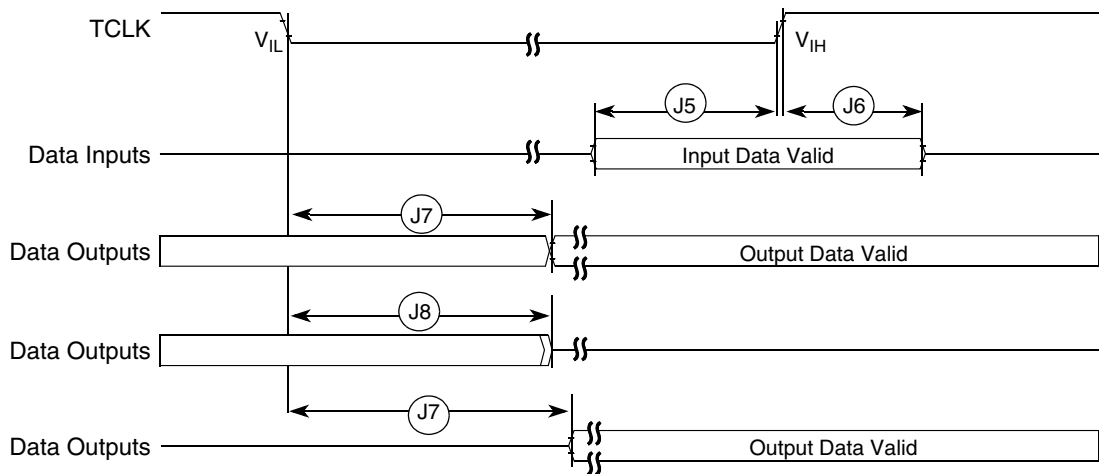
**Table 33. JTAG and Boundary Scan Timing (continued)**

Num	Characteristic <sup>1</sup>	Symbol	Min	Max	Unit
J9	TMS, TDI Input Data Setup Time to TCLK Rise	$t_{TAPBST}$	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	$t_{TAPBHT}$	10	—	ns
J11	TCLK Low to TDO Data Valid	$t_{TDODV}$	0	26	ns
J12	TCLK Low to TDO High Z	$t_{TDODZ}$	0	8	ns
J13	$\overline{TRST}$ Assert Time	$t_{TRSTAT}$	100	—	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	$t_{TRSTST}$	10	—	ns

<sup>1</sup> JTAG\_EN is expected to be a static signal. Hence, specific timing is not associated with it.



**Figure 29. Test Clock Input Timing**



**Figure 30. Boundary Scan (JTAG) Timing**

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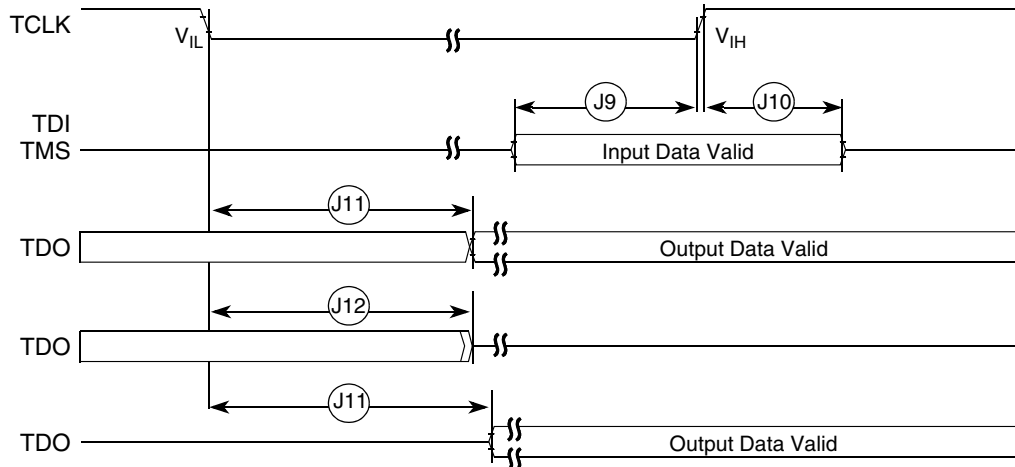
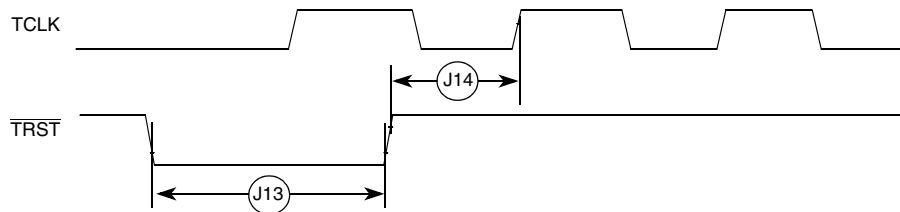


Figure 31. Test Access Port Timing

Figure 32.  $\overline{\text{TRST}}$  Timing

## 5.18 Debug AC Timing Specifications

Table 34 lists specifications for the debug AC timing parameters shown in Figure 33.

Table 34. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1	1	$t_{\text{sys}}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4 <sup>1</sup>	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

<sup>1</sup> DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

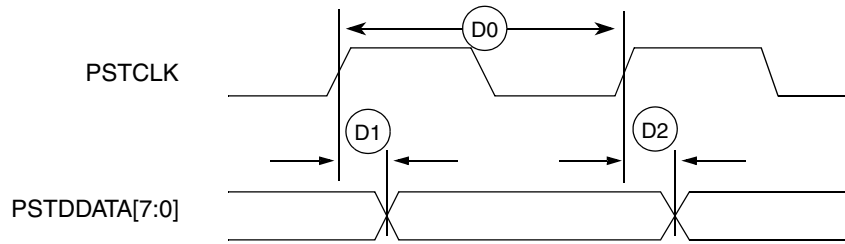


Figure 33. Real-Time Trace AC Timing

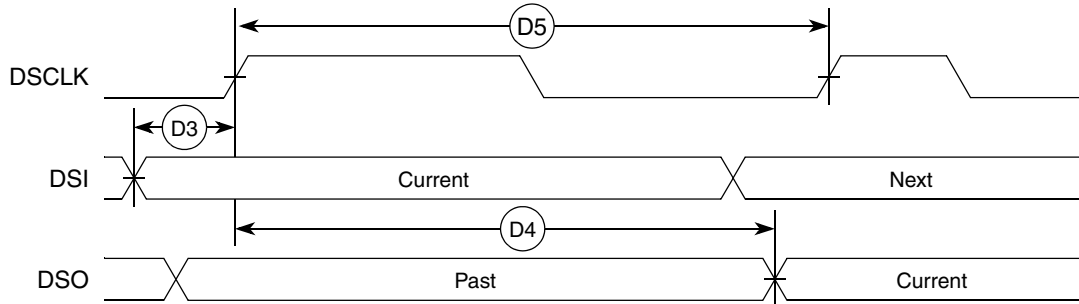


Figure 34. BDM Serial Port AC Timing

## 6 Package Information

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Table 35. Package Information

Device	Package Type	Case Outline Numbers
MCF52274	176 LQFP	98ASS23479W
MCF52277	196 MAPBGA	98ASH98061A

## 7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at <http://www.freescale.com/coldfire>.

## 8 Revision History

Table 36 summarizes revisions to this document.

**Table 36. MCF52277 Data Sheet Revision History**

Rev. No.	Date of Release	Summary of Changes
3	02/2008	Initial public revision.
4	05/2008	Corrected MCF52274 order number from MCF52274CAB120 to MCF52274CLU120 in <a href="#">Table 2</a>
5	07/2008	Corrected MCF52277CVM166 part number to MCF52277CVM160 in <a href="#">Table 2</a> . Although, this device has a maximum rated frequency of 166.67 MHz.
6	07/2008	Added data to <a href="#">Section 3.5, "Power Consumption Specifications."</a>

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